List of Figures

Figure No.	Name of Figure	Page No.
2.1	Wireless Networks: Taxonomy	10
2.2	TRUETIME library block	17
2.3	Simplified User's View of NS	18
2.4	Architectural View of NS	19
2.5	TRACE files Format	22
2.6(a)	Topology of the network in NAM	25
2.6(b)	Packet drops in queue of network (in NAM)	29
2.7	5 wireless node topology in NS2	29
2.8	Nam Output Of The Wirelesstest2.Tcl File	35
3.1	Ad hoc Routing Protocols – Classification	42
3.2	Scenario Created For Wireless Ad-Hoc Network in Qualnet	52
3.3	Information packet exchange between the nodes of the network in Qualnet	53
3.4	Average Packet Delivery Ratio V/S Maximum Speed and node density	54
3.5	Average end to end Delay V/S Maximum Speed and node density	55
3.6	Average Throughput V/S Maximum Speed and node density	55
3.7	Average Jitter V/S Maximum Speed and node density	56
3.8	Average Packet Delivery Ratio V/S Maximum Speed and node density	57
3.9	Average end to end Delay V/S Maximum Speed and node density	58
3.10	Average Throughput V/S Maximum Speed and node density	58
3.11	Average Jitter V/S Maximum Speed and node density	59
3.12	Average Packet Delivery Ratio V/S Mobility	60

3.13	Average Packet Delivery Ratio V/S Node Density	60
3.14	Average end to end Delay V/S Mobility	61
3.15	Average end to end Delay V/S node density	61
3.16	Average Throughput V/S Mobility	61
3.17	Average Throughput V/S node density	61
3.18	Average Jitter V/S Mobility	62
3.19	Average Jitter V/S node density	62
3.20	Average Packet Delivery Ratio V/S Mobility	63
3.21	Average Packet Delivery Ratio V/S node density	63
3.22	Average end to end Delay V/S Mobility	63
3.23	Average end to end Delay V/S node density	63
3.24	Average Throughput V/S Mobility	64
3.25	Average Throughput V/S node density	64
3.27	Average Jitter V/S Mobility	65
3.28	Average Jitter V/S node density	65
4.1	The Architecture of Fuzzy Inference System	72
4.2	Simple model of an Artificial Neuron	75
4.3	Multi-layer Network	77
4.4	ANFIS Architecture	91
4.5(a)	A Schematic Diagram Of Main Features: MATLAB	93
4.5(b)	MATLAB command window	94
4.6	SIMULINK library browser window	95
4.7	ANFIS Editor GUI	97
5.1	Simulink model in Truetime	108
5.2	Topology created by Simulink model in Truetime	109

5.3	**Results on Command window for AODV Simulink model**	**110**
5.4	**Signal Reach v/s Tx Power**	**111**
5.5	**Packet delivery Ratio v/s Transmission Power**	**111**
5.6	**End to End delay (sec) v/s Power (dBm)**	**112**
5.7	**Rule Viewer**	**114**
5.8	**Surface Viewer**	**115**
5.9(a)	**Block schematic of ANFIS**	**115**
5.9(b)	**ANFIS model structure**	**116**
5.10	**Error v/s Epochs**	**117**
5.11	**Surface viewer for ANFIS**	**117**
5.12	**Comparisons between Simple AODV, Fuzzy AODV and ANFIS AODV**	**118**
5.13	**Parts of GUI implementation**	**119**
5.14	**User Interface for Application**	**120**
5.15	**GUI for password**	**121**
5.16	**GUI showing initialization**	**121**
5.17	**GUI showing node topology**	**122**
5.18	**Fuzzy AODV and ANFIS AODV**	**122**
5.19	**Various response for view menu**	**123**
5.20	**Response of PDR and results of workspace**	**123**
6.1	**the Route Request packets flooding in AODV**	**126**
6.2	**Forwarding of Route Reply packet in AODV**	**127**
6.3	**Fuzzy control Architecture**	**128**
6.4	**Fuzzy Inference System with respective inputs and outputs.**	**132**
6.5	**Membership Functions Selection for Fuzzy Inference System (Fuzzy AODV)**	**133**
6.5(a)	**MBF Library**	**133**

6.5(b)	**MBF Editor: FIS for Hello Interval (HI)**	**133**
6.6	**Surface Viewer for FIS Hello Interval (HI)**	**134**
6.7(a)	**Scenario Created For Wireless Ad-Hoc Network in Qualnet**	**135**
6.7(b)	**Scenario Created For Wireless Ad-Hoc Network in Qualnet**	**136**
6.8(a)	**Average Packet Delivery Ratio V/S Pause time for nodes 30**	**138**
6.8(b)	**Average Packet Delivery Ratio V/S Pause time for nodes 40**	**138**
6.9(a)	**Average Throughput V/S Pause Time for node 30**	**139**
6.9(b)	**Average Throughput V/S Pause Time for node 40**	**139**
6.10(a)	**Average Jitter V/S Pause Time for node 30**	**139**
6.10(a)	**Average Jitter V/S Pause Time for node 40**	**139**
6.11(a)	**Average Received Packets V/S Pause Time for nodes 30**	**140**
6.11(b)	**Average Received Packets V/S Pause Time for nodes 40**	**140**
7.1	**A learning Cycle in the ANN model**	**143**
7.2(a)	**ANN with respective inputs and outputs**	**146**
7.2(b)	**ANN layered Architecture with neurons**	**146**
7.3	**Process of Optimization of MANET**	**147**
7.4	**Training of Artificial Neural Network Hello Interval (HI)**	**148**
7.5(a)	**Average Packet Deelivery Ratio V/S Pause Time for nodes 30**	**149**
7.5(b)	**Average Packet Deelivery Ratio V/S Pause Time for nodes 40**	**149**
7.6(a)	**Average Throughput V/S Pause Time for nodes 30**	**149**
7.6(b)	**Average Throughput V/S Pause Time for nodes 40**	**149**
7.7(a)	**Average End to End Delay V/S Pause Time for node 30**	**150**
7.7	**Average End to End Delay V/S Pause Time for node 40**	**150**
7.8(a)	**Received Packets V/S Pause Time for node 30**	**150**
7.8 (b)	**Received Packets V/S Pause Time for node 40**	**150**

7.9	Genetic Tuning Algorithm	152
7.10	Schemes for Training a Neural Network to Identify a Plant	156
7.11	Weights of Each Layer of ANN	157
7.12	Arrangement of Weights and Biases in the GA Chromosome	157
7.13	Flow Chart of the Proposed Algorithm	159
8.1	Process of FPGA Based ANN for Reactive Routing Protocol for MANET	169
8.2	System Block Diagram of FPGA Implementation of ANN AODV	170
8.3(a)	Output of Purelin ANN from ISIM Using VHDL code	171
8.3(b)	Output of Tansig ANN from ISIM Using VHDL code	172
8.4(a)	Relative difference of Purelin type ANN	173
8.4(b)	Relative difference of Tansig type ANN	173
8.5(a)	Hardware setup of FPGA Implementation of ANN based HI	174
8.5(b)	Hardware Setup of FPGA implementation of ANN	175
8.5(c)	Enlarge View of FPGA Board in Hardware Setup	175
8.6(a)	Snap Shot of Output of Purelin ANN on Logic Analyzer	176
8.6(b)	Snap Shot of the output of Tansig ANN observed on GPIO pins using Logic Analyzer	176
8.7	Hardware Setup of FPGA implementation of ANN with LCD	177
8.8(a)	Snap Shot of Tansig type ANN Input and Outputs Are Displayed on LCD	177
8.8(b)	Snap Shot of Tansig type ANN Input and Outputs Are Displayed on LCD	178
8.9	Block Schematic of ANFIS	181
8.10	Internal architecture of ANFIS	182
8.11	Training data loaded for ANFIS	182
8.12	Training Error of ANFIS for Hello Interval (HI)	182
8.13	Average Packet Delivery Ratio V/S Pause time for nodes 30, 40	183
8.14	Average Throughput V/S Pause Time for nodes 30, 40	183

8.15	**Average End to End Delay V/S Pause Time for nodes 30, 40**	**183**
8.16	**Average Received Packets V/S Pause Time for nodes 30, 40**	**183**
8.17	**Average comparison of performance metrics for nodes 30 and 40**	**184**
9.1(a)	**Relative Difference Of Purelin Type ANN**	**188**
9.1(b)	**Relative Difference Of Tansig Type ANN**	**188**
9.2	**Average Packet Delivery Ratio V/S Pause Time Of Nodes 40**	**189**
9.3	**Average End To End Delay V/S Pause Time Of Nodes 40**	**189**
9.4	**Average Throughput V/S Pause Time Of Nodes 40**	**190**
9.5	**Average Jitter V/S Pause Time Of Nodes 40**	**190**
9.6	**Average Number Of Received Packets V/S Pause Time Of Nodes 40**	**190**
9.7	**Average Packet Delivery Ratio V/S Pause Time Of Nodes 30**	**191**
9.8	**Average End To End Delay V/S Pause Time Of Nodes 30**	**191**
9.9	**Average Throughput V/S Pause Time Of Nodes 30**	**191**
9.10	**Average Jitter V/S Pause Time Of Nodes 30**	**191**
9.11	**Average Number Of Received Packets V/S Pause Time Of Nodes 30**	**191**
A.1	**ISE Design flow**	**218**
A.2	**Snap Shot Of Xilinx ISE Design Suite Icon**	**222**
A.3	**New Project Wizard: Create New Project Page**	**223**
A.4	**New Project Wizard: Project Settings**	**223**
A.5	**Project Summary**	**224**
A.6	**Status of Source Files and Associations**	**224**
A.7	**Process Pane**	**225**
A.8	**ISim Properties Dialog Box**	**225**
A.9	**ISim Graphical User Interface**	**226**
A.10	**Wave Window**	**226**

A.11(a)	**snap shot of boundary scan and adding Xilinx devices**	**228**
A.11(b)	**snap shot of boundary scan after adding Xilinx devices**	**229**
A.12	**PROGRAM Launch window**	**229**
A.13(a)	**Snap Shot of XCV5LX110T FPGA Board**	**231**
A.13(b)	**Snap Shot of XCV5LX110T FPGA Board with peripherals**	**231**
C-I	**WANET: Power Control by SOFTAODV User Interface**	**239**
C-II	**WANET: Power Control by SOFTAODV User Interface, Documentation**	**239**
C-III	**WANET: Power Control by SOFTAODV User Interface, SOFT_AODV Menu**	**240**
C-IV	**WANET: Power Control by SOFTAODV User Interface, Hardware implementation**	**240**
C-V	**WANET: Power Control by SOFTAODV User Interface, DEMO**	**241**
C-VI	**WANET: Power Control by SOFTAODV User Interface, Help**	**241**