

PUBLICATIONS

1. J.G. Jamnani, S. A. Kanitkar, "Design, Simulation and Comparison of Synthetic test circuits for High Voltage Circuit Breakers" International Conference on power system Technology 2008 (POWERCON 2008) & 2008 IEEE Power India Conference held during October 12-15, 2008 at New Delhi.
2. J.G.Jamnani, S.A.Kanitkar , "Computer Aided Optimized Design, Simulation and Comparison of Synthetic Test Circuits For 245kV Rating Circuit Breakers" International Journal of Engineering and Technology , IETECH Journal of Electrical Analysis, Vol.2, No.4, pp.258-262, Nov. 2008.
3. J.G. Jamnani, S.A.Kanitkar , "Development and Fabrication of Automatic Controller and Triggering Circuit for Circuit Breakers Synthetic Test Circuit" at 15th National Power System Conference (NPSC-2008) held at IIT , Bombay during Dec.16-18 2008, pp.37-42.
4. J.G. Jamnani, S.A.Kanitkar , " Design, Simulation and Comparison of Synthetic test circuits for Extra High Breakers" IET-International Conference on Information and communication Technology in Electrical Sciences (ICTES-2007) held during Dec. 20 - 22, 2007 at Chennai, pp.464-468.
5. J.G. Jamnani, S.A.Kanitkar "Design and Simulation of 2- Parameters TRV synthetic testing circuits for Medium voltage circuit breakers" IEEE International Conference on Electrical Engineering, (ICECE-2006) held during Dec.19-21, 2006 at Dhaka, Bangladesh, pp.1-4.
6. J.G. Jamnani, S.A.Kanitkar , " Design and Simulation of 4 - Parameters TRV synthetic testing circuits for High Voltage circuit breakers" IEEE International Conference on Electrical Engineering (ICECE-2006) held during Dec.19-21, 2006 at Dhaka, Bangladesh, pp. 25-28.

7. J.G. Jamnani, S.A.Kanitkar, “ Review of synthetic testing circuits for medium and high voltage circuit breakers” at National conference on power system Engg. PSE-06, Sri Ramakrishna Engg. College, Coimbatore, Nov. 2006.
8. J.G. Jamnani, S.A.Kanitkar , “ Analysis and computer aided design of synthetic testing circuits for high voltage circuit breakers” at National conference on current trends in technology , NUCONE-2006, Institute of Technology, Nirma University , Ahmedabad, pp.235-238,Dec.2006.

Papers Accepted

1. J.G.Jamnani, S.A.Kanitkar, “Computer Aided Optimized Design, Simulation and Comparison of Synthetic Test Circuits For 420 kV Rating Circuit Breakers”, at 2009 IEEE PES power systems conference held at Seattle Washington USA during March 15-18,2009.
2. J.G.Jamnani, S.A.Kanitkar, “Computer Aided Optimized Design and Simulation of Synthetic Test Circuit for Testing 800kV Rating Circuit Breakers” IEEE International conference on Emerging Technologies for sustainable development (TENCON2009) to be held at Singapore during November 23-26,2009
