CHAPTER 2

MULTILEVEL INVERTER to HYBRID MULTILEVEL INVERTER

This chapter gives comparative study of multilevel inverters and evolution of hybrid multilevel inverter.

The idea of multilevel inverters has been introduced since 1975 [1]. The term multilevel began with three level inverter [2]. Thereafter several multilevel inverter topologies have been developed [3–9]. But the basic concept of a multilevel inverter is to obtain high power by using a series of power semiconductor switches. Thus a staircase voltage waveform can be achieved from several low voltage DC sources. Capacitors, batteries and renewable energy voltage sources can be used as the multiple DC voltage sources. The switching of the power switches combine these multiple DC sources in order to achieve high voltage at the output however the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected.

A multilevel inverter achieves high power ratings and also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for a high power application [10-12]. Thus a multilevel power inverter structure can be utilized as an alternative in high power and medium voltage situations. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM).

2.1 MULTILEVEL INVERTER CONFIGURATION

Many multilevel inverter topologies have been proposed during the last three decades. Modern research has engaged novel inverter topologies and unique modulation schemes. Three different major multilevel inverter structures have been reported in the literature: cascaded H-bridges inverter with separate DC sources, diode clamped (neutral clamped) and flying capacitors (capacitor clamped).

The first topology introduced was the series H-bridge design [1]. This was followed by the diode-clamped multilevel inverter [2,14,15] which utilizes a bank of series capacitors to split the DC bus voltage. After few years the flying-capacitor (or capacitor clamped) [16] topology was introduced in which instead of series connected capacitors floating capacitors are used to clamp the voltage levels. Another multilevel design, slightly different from the previous ones, involves parallel connection of inverter outputs through inter-phase reactors [17]. In this design the switches must block the entire reverse voltage, but share the load current. Various combinatorial designs have

also emerged [18] and been implemented by cascading the fundamental topologies [19-23] such designs come under hybrid topologies category. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies due to a multiplying effect of the number of levels.

Moreover, number of modulation techniques and control techniques have been developed for multilevel inverters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), multicarrier modulation and others.

In the beginning multilevel inverters were introduced to drive high voltage as in High Voltage Direct Current (HVDC) applications to make the front-end connection between DC and AC lines. In this way the limits on the maximum voltage tolerable by the semiconductor switches were overtaken and the inverters were able to drive directly the line voltage without a transformer.

Nowadays it is possible to find multilevel applications even in low voltage field like motor drive because of the high quality of the AC output. In particular back-to-back multilevel systems can drive motors with very good performance concerning the line voltage and current distortions and also reduces the losses. Recent advances in power electronics have made the multilevel concept practical [2, 14-30]. In fact the concept is so advantageous that several major drive manufacturers have obtained patents on multilevel power inverter and associated switching techniques [4, 31-36].

In addition, many multilevel inverter applications focus on industrial medium-voltage motor drives [7, 37] utility interface for renewable energy systems [38] flexible ac transmission system (FACTS) [39] and traction drive systems.

2.1.1 WORKING PRINCIPLE OF MULTILEVEL INVERTER

General concept of multilevel inverter can be explained in this section which is very popular. In this explanation operation of semiconductors are shown by an ideal switch with several states. The switching pattern of switches and commutation of them allow the addition of the capacitor voltages as temporary DC voltage sources whereas the switches should withstand the voltages of capacitors. Thus Fig. 2.1 shows one phase leg of multilevel inverter with different number of levels [10].

Fig. 2.1(a) is a two-level inverter since the output voltage V_a has only two possible values while Fig. 2.1(b) is a three-level inverter since its output can have three different values. If m is the number of possible output voltage levels it is called m-level inverter shown in Fig. 2.1(c). By increasing the number of levels the output voltage

waveforms will have more steps and thus have a reduced harmonic distortion. However a high number of levels will increase the complexity and introduce voltage imbalance problems.

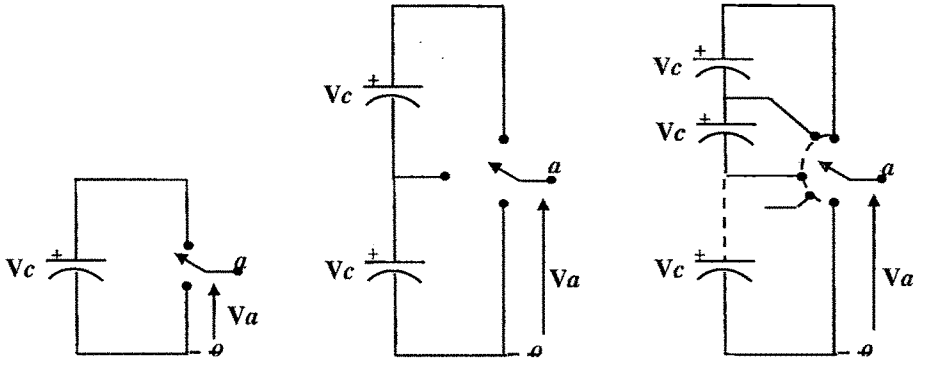


Fig. 2.1 Single leg of multilevel inverter (a) Two level (b) Three level (c) m level

2.2 DIODE CLAMPED MULTILEVEL INVERTER

Fig. 2.2 describes working of a three-level diode-clamped inverter. In this circuit two series-connected bulk capacitors C_1 and C_2 divide the DC-bus voltage. If the middle point of the two capacitors is defined as the neutral point n then the output voltage v_{an} has three states: $V_{dc}/2$, 0 and - $V_{dc}/2$. When switches S_1 and S_2 are turned on then output voltage v_{an} is $V_{dc}/2$ while for – $V_{dc}/2$ output switches S_1'and S_2' are turned on and for the 0 level S_2 and S_1' are switched on.

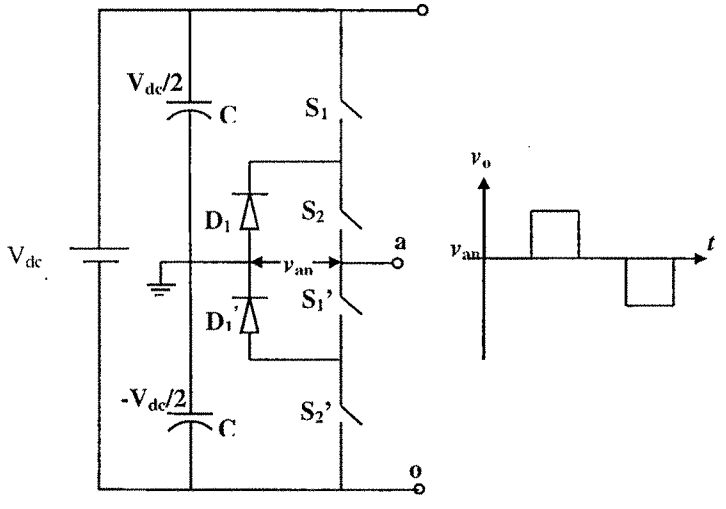


Fig. 2.2 Three level diode clamped inverter

The key components that distinguish this circuit from a conventional two-level inverter are diodes D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the DC-bus voltage. When both switches S_1 and S_2 turn on the voltage across '*a*' and 'o' is V_{dc} i.e. $V_{ao}=V_{dc}$. In this case D_1' balances the voltage sharing between S_1'and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Note that output voltage v_{an} is ac and V_{ao} is DC. The difference between v_{an} and V_{ao} is the voltage across C_2 which is $V_{dc}/2$. If the output is between '*a*' and 'o', then the circuit becomes a DC/DC inverter which has three output voltage levels: V_{dc}, $V_{dc}/2$ and 0.

Fig. 2.3 shows a five-level diode-clamped inverter in which the DC bus consists of four capacitors C_1, C_2, C_3 and C_4. For DC-bus voltage V the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level i.e. $V_{dc}/4$ through clamping diodes.

To explain how the staircase voltage is obtained the neutral point '*n*' is considered as the output phase voltage reference point. There are five switch combinations to obtain five level voltages across '*a*' and '*n*'.

For voltage level $v_{an}=V_{dc}/2$ turn on all upper switches S_1–S_4. For voltage level $v_{an}=0$, turn on two upper switches S_3 and S_4 and two lower switches S_1' and S_2'. For voltage level $v_{an}=-V_{dc}/4$ turn on one upper switch s4 and three lower switches S_1'–S_3'. Similarly it can be explained for other voltage levels. Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1, S_1'), (S_2, S_2'), (S_3,S_3'), and (S_4,S_4').

Although each active switching device is only required to block a voltage level of V_{dc}/ (m-1), the clamping diodes must have different voltage ratings for reverse voltage blocking. Using D_1' of Fig. 2.3 as an example when lower devices S_2'-S_4'are turned on, D_1' needs to block three capacitor voltages or $3V_{dc}/4$. Similarly D_2 and D_2' need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m-1)x(m-2). This number represents a quadratic increase in m. When m is sufficiently high the number of diodes required will make the system impractical to implement. If the inverter runs under PWM the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications [10].

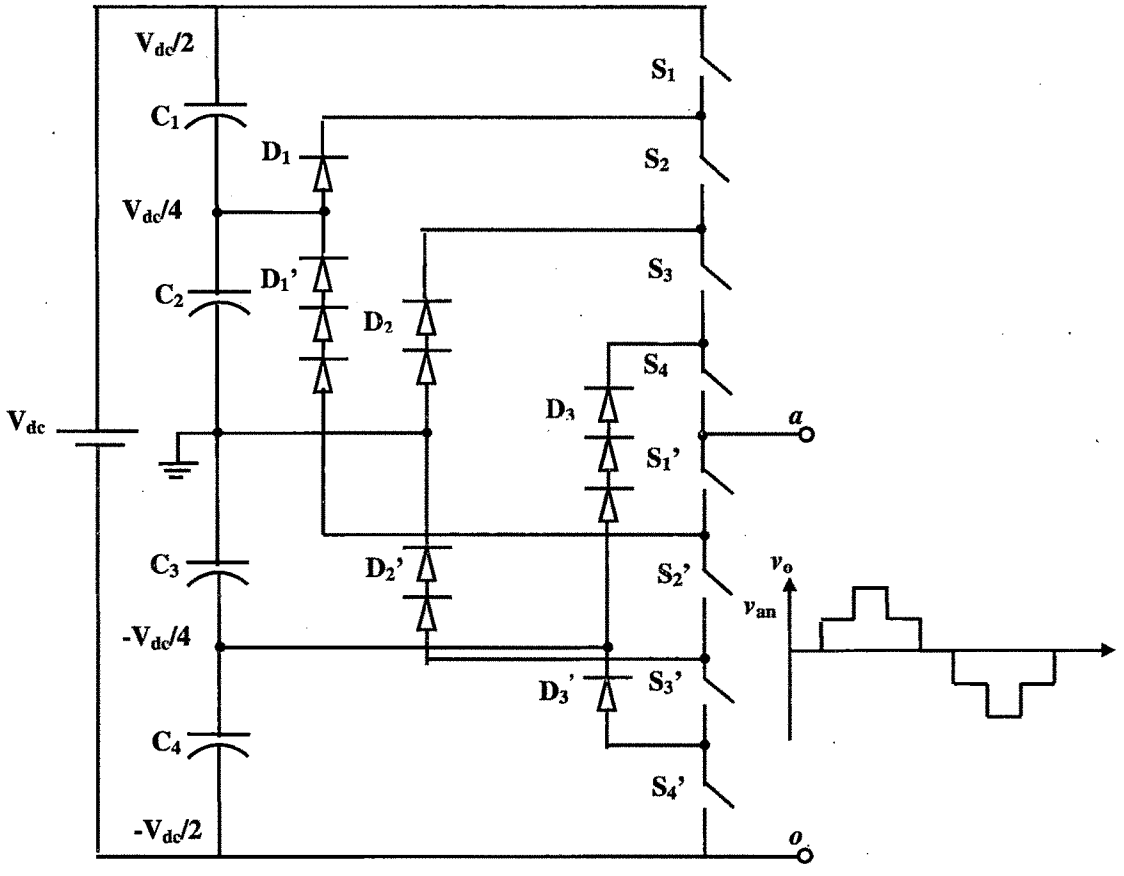


Fig. 2.3 Five level diode clamped inverter

Table 2.1 Switching combination for five level DCMLI

SWITCHING STATES								Output Voltage
S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	
ON	ON	ON	ON	OFF	OFF	OFF	OFF	$V_{dc}/2$
OFF	ON	ON	ON	ON	OFF	OFF	OFF	$V_{dc}/4$
OFF	OFF	ON	ON	ON	ON	OFF	OFF	0
OFF	OFF	ON	ON	ON	ON	ON	OFF	$-V_{dc}/4$
OFF	OFF	OFF	OFF	ON	ON	ON	ON	$-V_{dc}/2$

2.3 FLYING CAPACITOR MULTILEVEL INVERTER

Fig.2.4 illustrates the fundamental building block of single phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter [11], [16], [40] with independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig. 2.4 provides a three-level output across *a* and *n*, i.e. v_{an} =$V_{dc}/2$, 0 or – $V_{dc}/2$. For voltage level $V_{dc}/2$ switches S_1 and S_2 need to be turned on for $-V_{dc}/2$ switches S_1'and S_2' need to be turned on and for the 0 level either pair (S_1,S_1') or

(S_2,S_2') needs to be turned on. Clamping capacitor C_1 is charged when S_1 and S_2' are turned on and is discharged when S_2 and S_1' are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination.

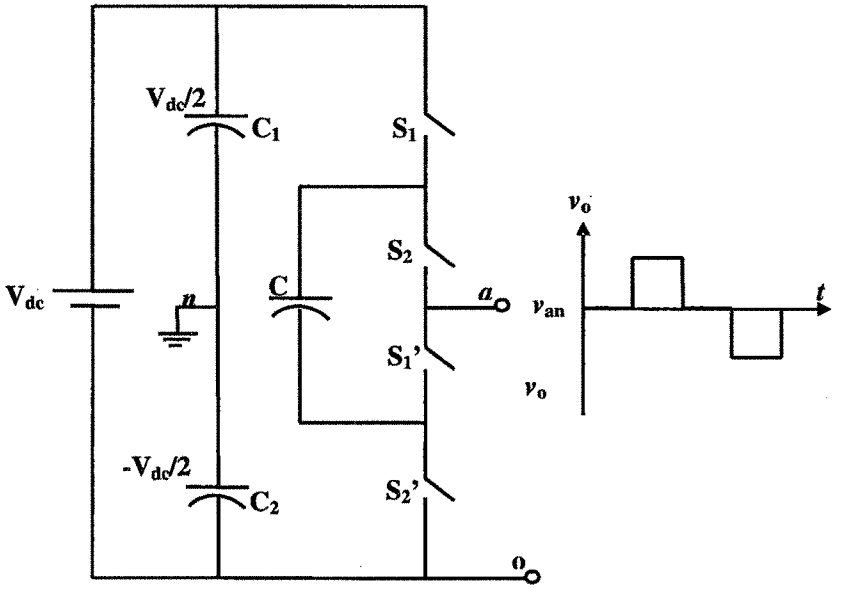


Fig. 2.4 Three level flying capacitor multilevel inverter

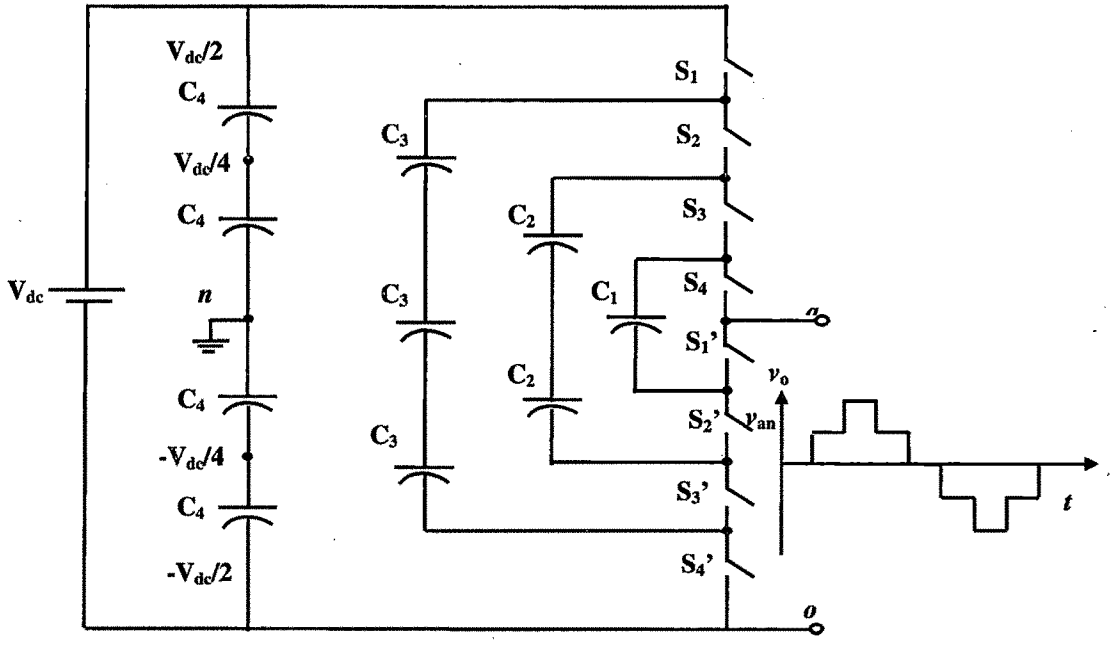


Fig. 2.5 Five level flying capacitor multilevel inverter

The voltage synthesis in a five-level capacitor-clamped inverter has more flexibility than a diode-clamped inverter. Using Fig. 2.5 as an example the voltage of the five-level phase-leg '*a*' output with respect to the neutral point '*n*', v_{an} can be obtained by following switching combinations.

Table 2.2 Switching combination for five level FCMLI

SWITCHING STATES								Output Voltage
S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	
ON	ON	ON	ON	OFF	OFF	OFF	OFF	$V_{dc}/2$
ON	ON	ON	OFF	ON	OFF	OFF	OFF	$V_{dc}/4$
OFF	ON	ON	ON	OFF	OFF	OFF	ON	$V_{dc}/4$
ON	OFF	ON	ON	OFF	OFF	ON	OFF	$V_{dc}/4$
ON	ON	OFF	OFF	ON	ON	OFF	OFF	0
OFF	OFF	ON	ON	OFF	OFF	ON	ON	0
ON	OFF	ON	OFF	ON	OFF	ON	OFF	0
ON	OFF	OFF	ON	OFF	ON	ON	OFF	0
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	ON	OFF	OFF	ON	0
ON	ON	OFF	OFF	OFF	ON	ON	OFF	$-V_{dc}/4$
OFF	OFF	OFF	ON	OFF	ON	ON	ON	$-V_{dc}/4$
OFF	OFF	ON	OFF	ON	OFF	ON	ON	$-V_{dc}/4$
OFF	OFF	OFF	OFF	ON	ON	ON	ON	$-V_{dc}/2$

For voltage level $v_{an} = V_{dc}/2$, turn on all upper switches S_1– S_4. For voltage level $v_{an} = 0$, there are six combinations as shown in Table 2.2. For voltage level $v_{an} = -V_{dc}/4$ there are three combinations: S_1,S_1',S_2',S_3'($v_{an} = V_{dc}/2$ of upper C_4's $-3V_{dc}/4$ of C_3's), S_4,S_2',S_3',S_4'($v_{an} = V_{dc}/4$ of $C_1 - V_{dc}/2$ of C_4's) and S_3,S_1',S_3', S_4'($v_{an} = V_{dc}/2$ of C_2's – $V_{dc}/4$ of $C_1 - V_{dc}/2$ of lower C_4's). Other output voltage combinations are given in Table 2.2.

In the preceding description the capacitors with positive signs are in discharging mode while those with negative sign are in charging mode. By proper selection of capacitor combinations it is possible to balance the capacitor charge. Similar to diode clamping the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level inverter will require a total of (m-1)x(m-2)/2 clamping capacitors per phase leg in addition to (m-1) main DC-bus capacitors.

2.4 CASCADED MULTILEVEL INVERTERS

Inverter topology based on the series connection of single-phase inverters with separate DC sources [41] is explained here. As stated above, the general function of the multilevel inverter is to synthesize a desired voltage from several separate DC sources

(SDCSs) such as solar cells, fuel cells, ultra capacitors, etc. Fig. 2.6 shows the power circuit for one phase leg of a five-level inverter with two cells in each phase (one cell refers to single phase H Bridge).

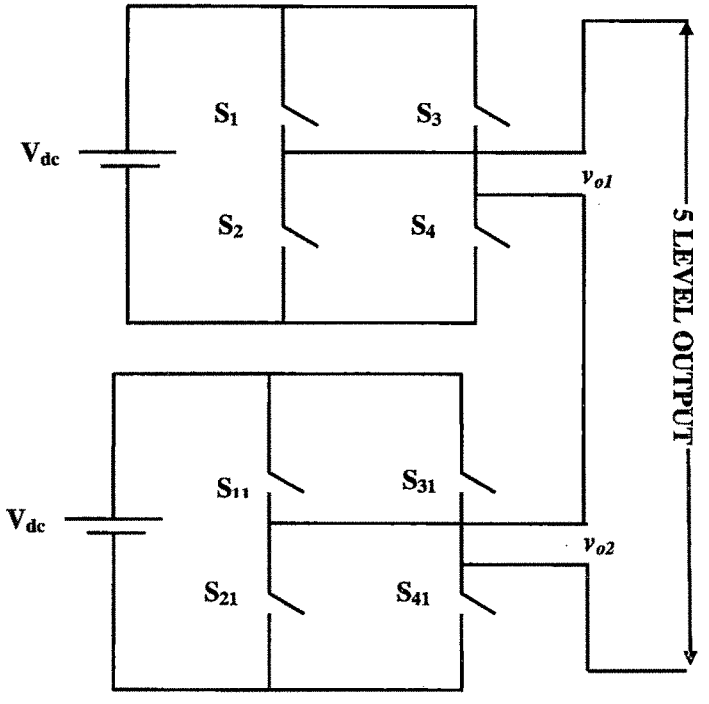


Fig. 2.6 Five level cascaded multilevel inverter

Table 2.3 Switching combination for five level CMLI

Switching State						Output Voltage v_{an}
S_{11}	S_{31}	S_{12}	S_{32}	V_{H1}	V_{H2}	
1	0	1	0	V_{dc}	V_{dc}	$2V_{dc}$
1	0	1	1	V_{dc}	0	V_{dc}
1	0	0	0	V_{dc}	0	V_{dc}
1	1	1	0	0	V_{dc}	V_{dc}
0	0	1	0	0	V_{dc}	V_{dc}
0	0	0	0	0	0	0
0	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0
1	0	0	1	V_{dc}	$-V_{dc}$	0
0	1	1	0	$-V_{dc}$	V_{dc}	0
0	1	1	1	$-V_{dc}$	0	$-V_{dc}$
0	1	1	0	$-V_{dc}$	0	$-V_{dc}$
1	1	1	1	0	$-V_{dc}$	$-V_{dc}$
0	0	0	1	0	$-V_{dc}$	$-V_{dc}$
0	1	0	1	$-V_{dc}$	$-V_{dc}$	$-2V_{dc}$

The resulting phase voltage is obtained by the addition of the voltages generated by the different cells.Each single-phase full-bridge inverter generates three voltages at the output: V_{dc}, 0 and $-V_{dc}$ this is accomplished by different combinations of the four switches in each cell as explained in Table 2.3. The ac output of each full-bridge inverter is connected in series such that the synthesized voltage waveform is the sum of all of the individual inverter outputs. The number of output phase (line-neutral) voltage levels in a cascade multilevel inverter is given by 2N+1, where N is the number of DC sources. The CHB inverter explained above can be extended to any number of voltage levels.

2.5 FEATURES OF MULTILEVEL INVERTER

Thus features of a multilevel inverter can be summarized as follows:

Output Waveform Quality: Multilevel inverters can generate the output voltages with very low distortion and reduced *dv/dt* stresses can be achieved therefore electromagnetic compatibility (EMC) problems can be minimized. Hence output waveform quality is improved.

Common-Mode (CM) Voltage: Multilevel inverters produce smaller CM voltage therefore the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [13]. Thus common mode voltage is reduced.

Input Current Distortion: Multilevel inverters can draw input current with low distortion.

Switching Frequency: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

High Voltage Capacity: Multilevel inverter structure can be utilized in high and medium voltage applications.

Low THD and *dv/dt*: The output waveform voltages is composed of voltage levels greater than three which leads to lower THD and dv/dt in comparison to the two-level inverter operating at the same voltage rating and device switching frequency.

Multilevel inverters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel inverter each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. Also the capacitor banks or insulated sources needed to achieve the voltage steps on the DC

busses.

2.6 HYBRID MULTILEVEL INVERTER

Hybrid multilevel inverter gives multi level operation by using hybrid source, hybrid configuration or hybrid device in such a way to produce output with reduced number of DC sources, high speed capability, low output switching frequency, low switching loss, high conversion efficiency, flexibility to enhance and various topologies for different applications.

Broadly HMLI can be classified as per power circuit configuration and modulation technique used.

2.7 CLASSIFICATION OF HYBRID MULTILEVEL INVERTER

Hybrid multilevel inverters are classified on basis of types of power devices used, number of power supplies used, magnitude of the power supplies used and how power devices are connected in circuit. Thus broad classification of hybrid multilevel inverter is as follows:

- ***Asymmetric Hybrid Multilevel Inverter***
- ***Hybrid Multilevel Inverter Based on Half-Bridge Modules***
- ***New Symmetrical Hybrid Multilevel Inverters***
- ***Hybrid Clamped Five-Level Inverter Topology***
- ***Distinct Series Connected cells Hybrid Multilevel Inverter***
- ***Hybrid Medium-Voltage Inverter based on a NPC Inverter***
- ***New Hybrid Asymmetrical Multilevel H-bridge Inverter***
- ***Hybrid Multilevel Inverter with Single DC Source***

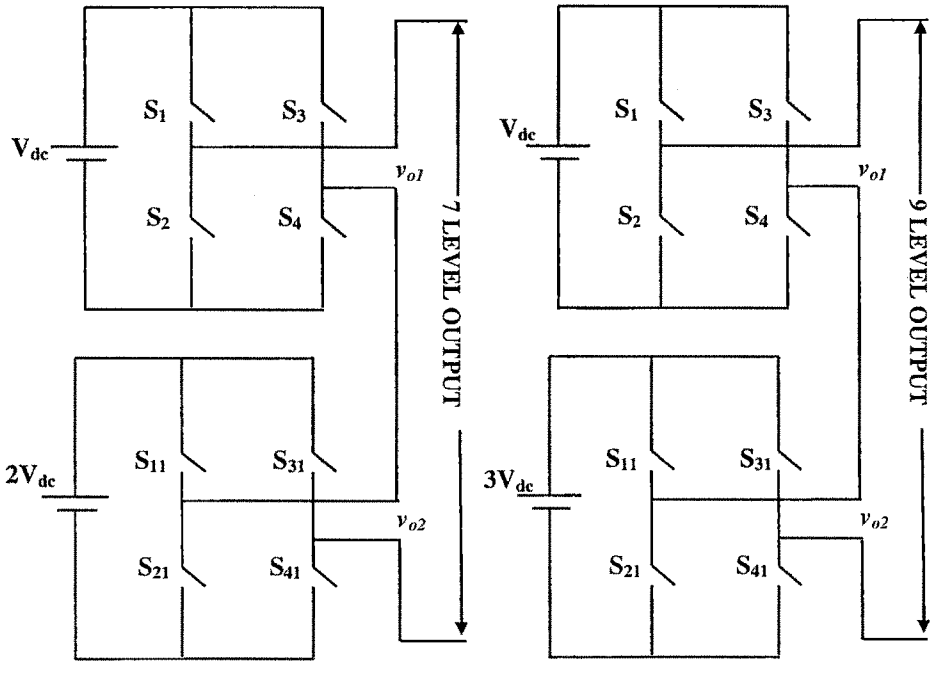
2.7.1 ASYMMETRIC HYBRID MULTILEVEL INVERTER [1,2]

In previous description of cascaded multilevel inverter the DC voltages of each cell are equal. However it is possible to have different voltage levels among the cells [42], [43] and such circuit is called as asymmetric hybrid multilevel inverter. Fig. 2.7 shows an example of two separate DC-bus levels one with low voltage switches and the other with high voltage switches. Switches S_1- S_4 are low voltage switches like IGBT and switches S_{11}- S_{41} are high voltage switches like GTO. With unequal DC voltages the number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This allows more voltage steps in the inverter output voltage waveform for a given number of power cells [42, 44].

[1]Hina B. Chandwani and Meeta K. Matnani "A review of hybrid multilevel inverter configurations and their comparison" is published Elixirjournal Elixir Power Elec. Engg, May 2012, pp. 8483-8486.

[2] Hina B. Chandwani and Meeta K. Matnani, "A review and comparative study of hybrid multilevel inverter configuration" is published Elixirjournal Elixir Power Elec. Engg July 2012, pp. 9690-9692

Depending on the availability of DC sources the voltage levels are not limited to a specific ratio. This feature allows more levels to be created in the output voltage and thus reduces the harmonic contents with less cascaded cells.



(a) (b)

Fig. 2.7 Asymmetric hybrid multilevel inverter (a) seven level (b) nine level

Fig. 2.7 shows two inverter topologies, where the DC voltages for the H bridge cells are not equal. In the seven-level topology the DC voltages for H bridge1 and H bridge2 are V_{dc} and $2V_{dc}$ respectively. The two-cell inverter leg is able to produce seven voltage levels: $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$. The relationship between the voltage levels and their corresponding switching states is summarized in Table 2.3. In the nine-level topology, the DC voltage of H bridge2 is three times that of H bridge1. All the nine voltage levels can be obtained by replacing the H bridge2 output voltage of v_{o2} = ± 2 V_{dc} in Table 2.4 with $v_{o2} = \pm 3$ V_{dc} and then calculating the inverter phase voltage.

There are some drawbacks associated with the CHB inverter using unequal DC voltages. The merits of the modular structure are essentially lost. In addition, switching pattern design becomes much more difficult due to the reduction in redundant switching states [44] Therefore, this inverter topology has limited industrial applications. Even with the same voltage level among them, it is also possible to use high-frequency PWM for

one cell, while the other switches at a lower rate. Fig. 2.7 shows an example with two different devices. The top full-bridge cell uses the insulated gate bipolar transistor (IGBT), and the low cell uses the gate-turn-off thyristor (GTO) as its switching device. The GTO-based cell switches at a lower frequency, typically the fundamental frequency, and the IGBT-based cell switches at a PWM frequency to smooth the waveform [42], [43].

Table 2.4 Switching states for AHMLI

Switching State				Output Voltage		
S_1	S_3	S_{11}	S_{31}	v_{o1}	v_{o2}	$v_o = v_{o1} + v_{o2}$
1	0	1	0	V_{dc}	$2V_{dc}$	$3V_{dc}$
1	1	1	0	0	$2V_{dc}$	$2V_{dc}$
0	0	1	0	0	$2V_{dc}$	
1	0	1	1	V_{dc}	0	V_{dc}
1	0	0	0	V_{dc}	0	
0	1	1	0	$-V_{dc}$	$2V_{dc}$	
0	0	0	0	0	0	0
0	0	1	1	0	0	
1	1	0	0	0	0	
1	1	1	1	0	0	
1	0	0	1	V_{dc}	$-2V_{dc}$	$-V_{dc}$
0	1	1	1	$-V_{dc}$	0	
0	1	0	0	$-V_{dc}$	0	
1	1	0	1	0	$-2V_{dc}$	$-2V_{dc}$
0	0	0	1	0	$-2V_{dc}$	
0	1	0	1	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$

2.7.2 HYBRID MULTILEVEL INVERTER BASED ON HALF-BRIDGE MODULES

Cascaded half-bridge inverters [45]–[49] employ half-bridge modules connected in series instead of the H Bridges. These inverters are one of the alternatives to the conventional cascaded H Bridge inverters. The modular multilevel inverter [45]–[48] employ series connections of pairs of half-bridge modules. These modules are connected in delta forming a three phase system and the capacitors of DC links do not need isolated DC supplies [45], [46] since the voltage across each half-bridge module DC link capacitor can be actively controlled. The hybrid cascaded half-bridge inverter [49] uses an alternative connection of half-bridge modules to eliminate the output DC level. The three phase system is reached through a Y connection. The modules are also connected in pairs and the inverter is able to provide just odd levels in the output phase voltages. This type of inverter requires a higher number of insulated DC sources for the same

number of levels of a CHB. However, lower active power levels are processed in the DC sources.

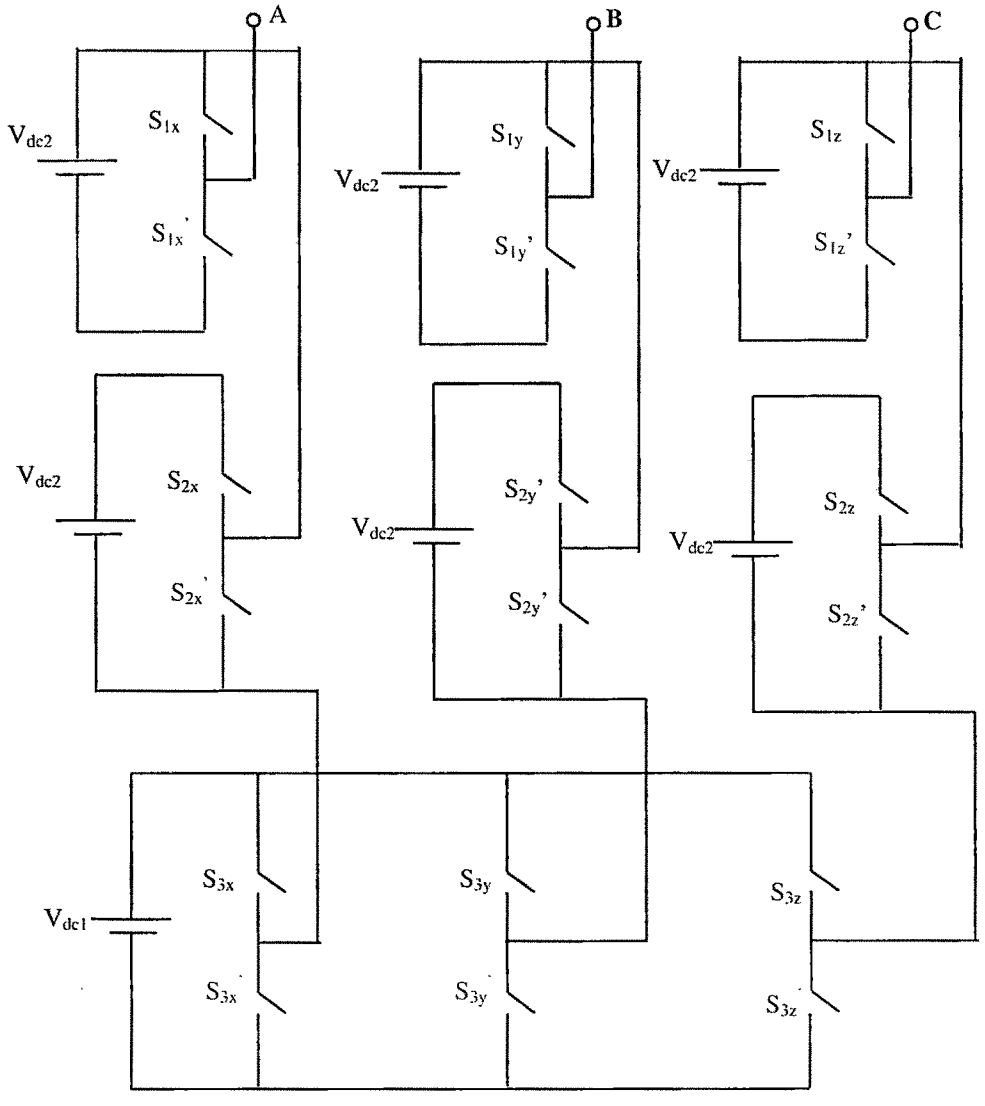


Fig. 2.8 Hybrid multilevel inverter based on half-bridge modules

This hybrid cascaded half-bridge inverter makes use of a three-phase inverter shown as a VSI in Fig. 2.8 where each output is series connected to a pair or multiple pairs (cascade) of half-bridge inverters connected with inverse polarity as shown in Fig. 2.8. Here the special connection of the half-bridge modules [49] guarantees that no DC level is observed at the output voltages. In the symmetrical version the modularity is preserved. Even though the number of insulated sources is increased for the same number of voltage

levels as for the CHB or HCHB this inverter lowers the ratings of these devices since the average current that is drawn from each 6-pulse rectifier feeding a half-bridge module is lower when compared to an H-bridge based inverter. Thus, higher power levels can be achieved for a given transformer/rectifier circuit. The assumptions made for the analysis of circuit are: (i) the switching devices are ideal (ii) the DC sources are constant positive voltages (iii) parasitics are neglected (iv) the virtual center point of the VSI's DC-link drawn in Fig. 2.8 is assumed as reference for the voltages.

It is observed that the output voltage v_A can assume six different values, which are given for v_o, with o = x;y;z, in Table 2.5. These output voltage levels depend on the DC sources voltages V_{dc2} and V_{dc1} and on the states of switches Sjo and Sjo0 , with j = 1; 2; 3. Based on these results, the hybrid cascaded half-bridge inverter can be operated with a number of levels N_{level} varying from four to six given that

$N_{level} = 4$; if $V_{dc2} = V_{dc1}$

$N_{level} = 5$; if $V_{dc2} = V_{dc1}/2$

$N_{level} = 6$; if $V_{dc1} \neq V_{dc2} \neq V_{dc1}/2$

Table 2.5 Resulting output phase voltage

S_{1o}	S_{2o}	S_{3o}	v_o	Case 1 $V_{dc2}=V_{dc1}=V_{dc}$	Case 2 $V_{dc2}=V_{dc1}/2=V_{dc}$	Case 3 $V_{dc2}=V_{dc1}/3=V_{dc}$
0	0	0	$-V_{dc2}-V_{dc1}/2$	$-3V_{dc}/2$	$-2V_{dc}$	$-5V_{dc}/2$
1	0	0	$-V_{dc1}/2$	$-V_{dc}/2$	$-V_{dc}$	$-3V_{dc}/2$
0	1	0	$-V_{dc1}/2$	$-V_{dc}/2$	$-V_{dc}$	$-3V_{dc}/2$
1	1	0	$V_{dc2}-V_{dc1}/2$	$+V_{dc}/2$	0	$-V_{dc}/2$
0	0	1	$-V_{dc2}+V_{dc1}/2$	$-V_{dc}/2$	0	$+V_{dc}/2$
1	0	1	$+V_{dc1}/2$	$+V_{dc}/2$	$+V_{dc}$	$+3V_{dc}/2$
0	1	1	$+V_{dc1}/2$	$+V_{dc}/2$	$+V_{dc}$	$+3V_{dc}/2$
1	1	1	$+V_{dc2}+V_{dc1}/2$	$+3V_{dc}/2$	$+2V_{dc}$	$+5V_{dc}/2$

2.7.3 NEW SYMMETRICAL HYBRID MULTILEVEL INVERTERS

With a proper driving pattern for switches $S_1 - S_4$, and for the switches of the H-Bridge, it is possible to obtain a voltage waveform between the points a-b as shown in Fig. 2.10. Then the circuit of Fig. 2.9 behaves as a five-level output voltage single-phase inverter. The single leg switches block voltages of value ' V_{dc}' and with proper modulation strategy they operate at high frequency (a few kHz). On the other hand, the H-bridge switches S_5, S_6, S_7 and S_8 must block a higher voltage level of '$2V_{dc}$'. However, these switches operate only in a semi cycle of the output voltage. Thus, they operate at low frequency commutating at zero voltage. Thus this inverter can also be classified among the hybrid multilevel inverters group.

As shown in [11] and [28], the multilevel inverters based on the H-bridge symmetrical cascade have a number of levels in its output voltage given by 2N+1. For circuit shown in Fig. 2.9 output voltage levels are also obtained through the same expression 2N+1 levels where N is the number of DC sources.

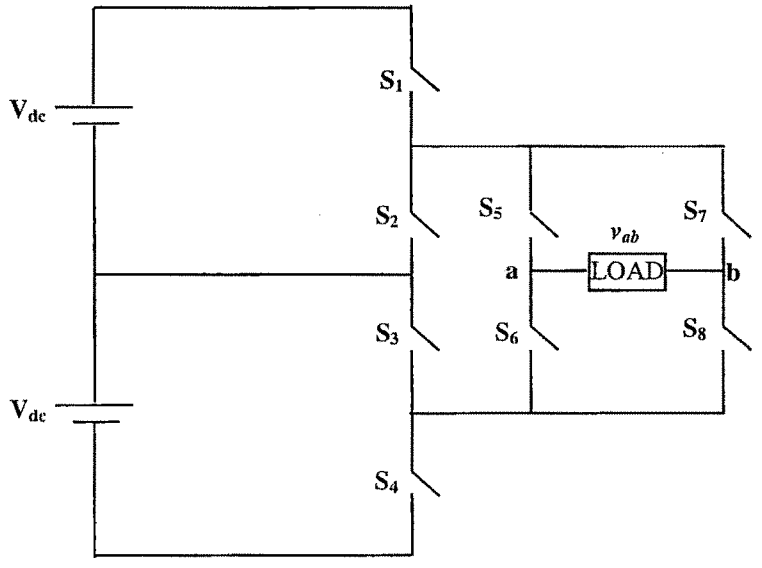


Fig. 2.9 New symmetrical hybrid multilevel inverter

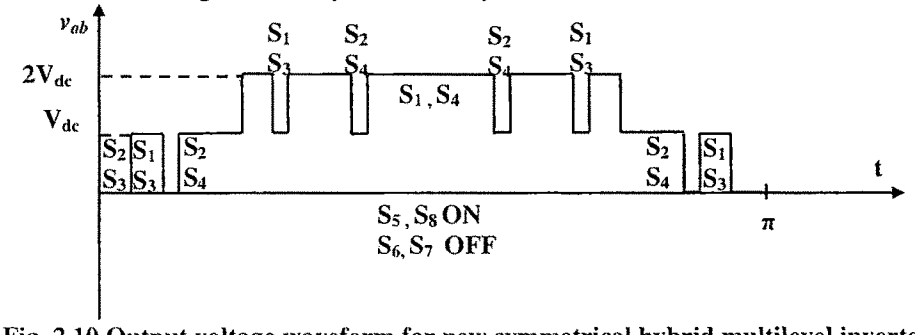


Fig. 2.10 Output voltage waveform for new symmetrical hybrid multilevel inverter

This can be implemented with the configuration shown in Fig. 2.9 where switches S_5 to S_8 are connected as a full-bridge inverter that is responsible for switching the load terminals according to the gate's signals. Fig. 2.10 shows the possible load voltage v_{ab} for the specified switching conditions. It is seen that the pairs S_5/S_8 and S_6/S_7 are turned on complementarily in order to generate, respectively, negative and positive voltages. The three-level DC–DC inverter switches S_1 to S_4 are switched according to a proper modulation pattern in order to generate a desired load voltage. Therefore, the inverter shown in Fig. 2.9 is a five-level single-phase inverter where switches S_1 to S_4

operate at high frequency and are rated for half of the DC-link voltage *E*. Switches S_5 to S_8 are rated for the full DC-link voltage $2V_{dc}$. On the other hand, switches S_5 to S_8 can be implemented with low-frequency devices such as GTOs, integrated gate commutated thyristors (IGCT), and others, since they switch a single time per load-voltage period under zero voltage. Based on this strategy, the proposed inverter is a symmetric (equal DC sources) hybrid (multiple carrier frequencies) multilevel inverter. Furthermore, the number of levels can be increased by cascading multiple single-phase inverters. This can be achieved with other topologies as well. As shown in [11] and [28], the total number of level across the load terminals v_{ab} for the mentioned topology is given by $v_{ab} = 2N + 1$ where N is the total number of DC sources

2.7.4 HYBRID CLAMPED FIVE-LEVEL INVERTER TOPOLOGY

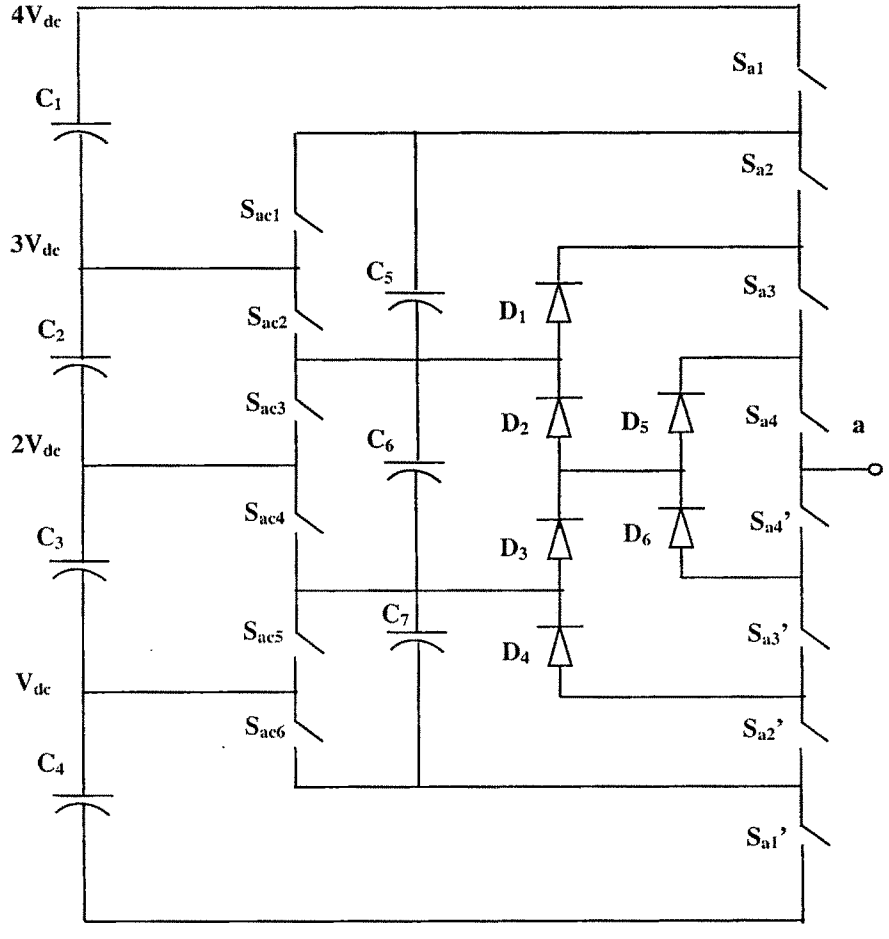


Fig. 2.11 Hybrid clamped five level inverter

A hybrid clamped multilevel inverter topology with self voltage balancing is discussed in

[50]. Fig. 2.11 shows one leg of the five-level topology. The main switching devices S_{a1}, S_{a2}, S_{a3} and S_{a4} are complementary with S_{a1}', S_{a4}', S_{a3}' and S_{a2}' respectively and S_{a1} is complementary with S_{ac1}.

Among the clamping switching devices S_{ac1} - S_{ac6} the adjacent switching devices are complementary. Self-voltage balancing in capacitors is realized by switching from one kind of device switching mode combination to another by turns.

Switching states are shown in Table 2.6 while Table 2.7 lists all the switching modes conversions for a hybrid clamped five-level inverter topology. From Table 2.7 it can be seen that there are two cases of switching modes conversions: (1) Switching modes conversions with the different output levels (2) Switching modes conversions with the same output levels. V_{dc} is equal to the voltage of one capacitor.

Table 2.6 Switching mode combinations

SWITCHING STATES				Output Voltage
S_1	S_2	S_3	S_4	
ON	ON	ON	ON	$2V_{dc}$
OFF	ON	ON	ON	V_{dc}
ON	OFF	ON	ON	V_{dc}
ON	OFF	OFF	ON	0
OFF	OFF	ON	ON	0
ON	ON	OFF	OFF	$-V_{dc}$
OFF	OFF	OFF	ON	$-V_{dc}$
OFF	OFF	OFF	OFF	$-2V_{dc}$

Table 2.7 Switching modes conversions for a hybrid clamped five-level inverter

Switching modes conversions	Output level conversions	Switching modes conversions	Output level conversions
1111→0111	$2V_{dc} \rightarrow V_{dc}$	1001→0011	$0 \rightarrow 0$
1111→1011	$2V_{dc} \rightarrow V_{dc}$	0011→0001	$0 \rightarrow -V_{dc}$
0111→1111	$V_{dc} \rightarrow 2V_{dc}$	1001→1000	$0 \rightarrow -V_{dc}$
1011→1111	$V_{dc} \rightarrow 2V_{dc}$	0001→0011	$-V_{dc} \rightarrow 0$
0111→1011	$V_{dc} \rightarrow V_{dc}$	1000→1001	$-V_{dc} \rightarrow 0$
1011→0111	$V_{dc} \rightarrow V_{dc}$	0001→1000	$-V_{dc} \rightarrow -V_{dc}$
0111→0C11	$V_{dc} \rightarrow 0$	1000→0001	$-V_{dc} \rightarrow -V_{dc}$
1011→1001	$V_{dc} \rightarrow 0$	0001→0000	$-V_{dc} \rightarrow -2V_{dc}$
0011→0111	$0 \rightarrow V_{dc}$	1000→0000	$-V_{dc} \rightarrow -2V_{dc}$
1001→1011	$0 \rightarrow V_{dc}$	0000→0001	$-2V_{dc} \rightarrow -V_{dc}$
0011→1001	$0 \rightarrow 0$	0000→1000	$-2V_{dc} \rightarrow -V_{dc}$

2.7.5 DISTINCT SERIES CONNECTED CELLS HYBRID MULTILEVEL INVERTER

In distinct series connected hybrid multilevel inverters two, three and five-level

cells connected in series as shown in Fig. 2.12[51]

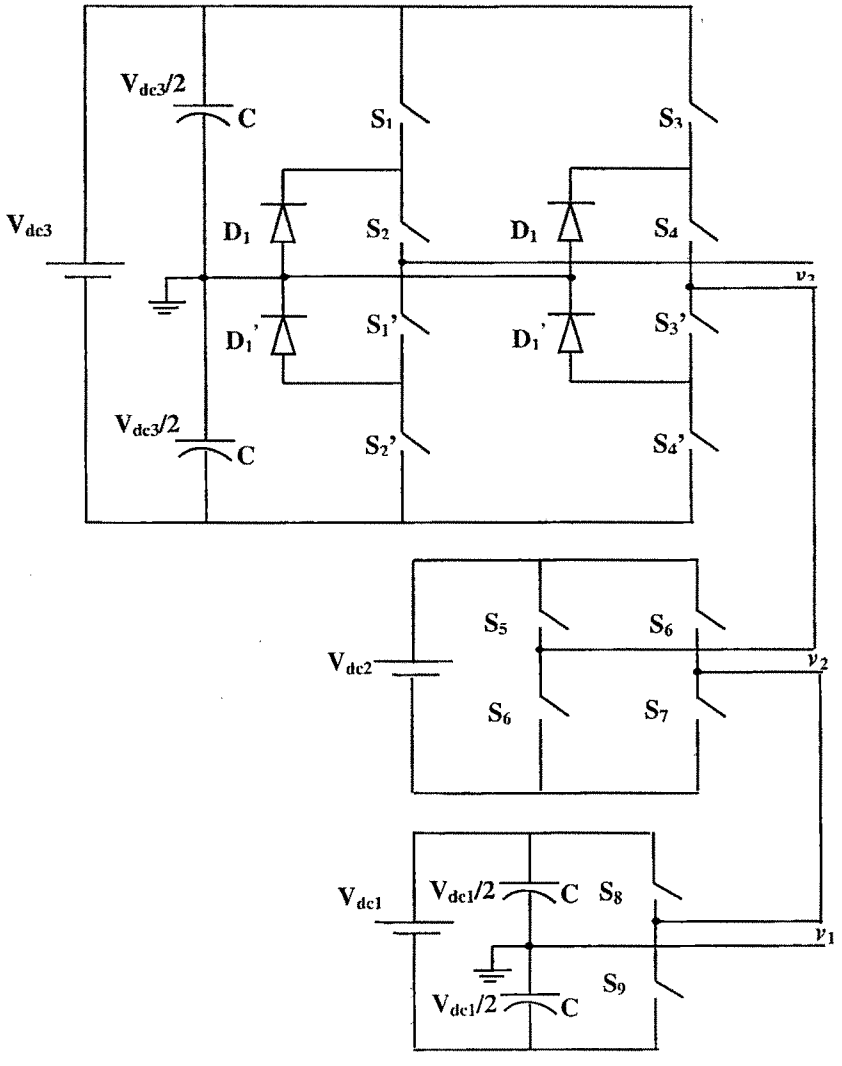


Fig. 2.12 Distinct series connected cells hybrid multilevel inverter

The first cell synthesizes two levels with 1-p.u. voltage step, the second cell generates three levels also with 1-p.u. voltage step and the third cell synthesizes five levels with 3-p.u. voltage steps. The switching devices of the two-level cell operate at high frequency, while the switches that compose the five-level cell operate at fundamental frequency. As v_1, v_2, and v_3 satisfy equation, the phase-voltage waveform with 16 levels is modulated at high frequency among any adjacent levels.

$$v_j \leq \sum_{k=1}^{j-1} (m_{k-1}) V_k$$

This example demonstrates the wide variety of arrangements that can be adopted to obtain a given number of levels. Thus it is essential to develop a design methodology to define the main parameters of a hybrid inverter such as the number of series-connected cells DC voltage levels and topologies used in each cell.

2.7.6 MEDIUM-VOLTAGE HYBRID MULTILEVEL INVERTER BASED ON A NPC INVERTER

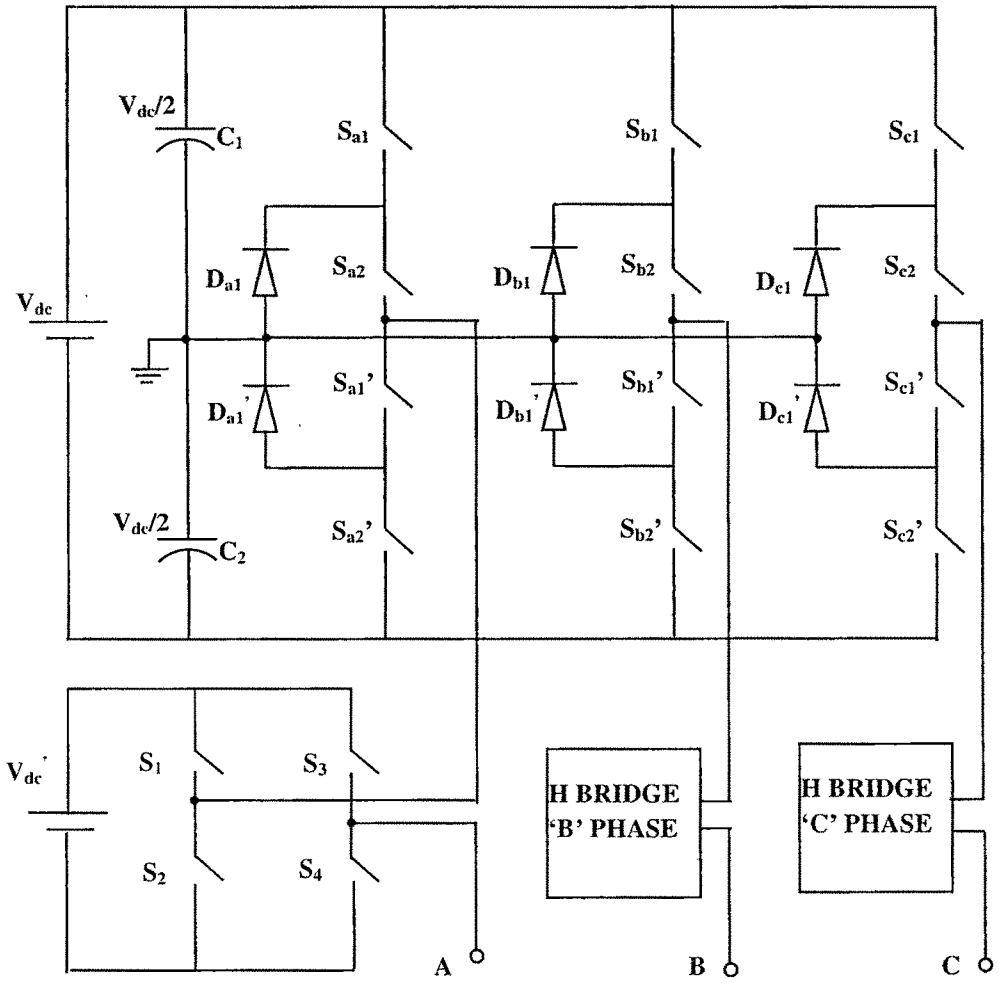


Fig. 2.13 Hybrid medium voltage inverter based on NPC inverter

This hybrid topology is composed of a traditional three-phase three-level NPC inverter and single phase H bridge inverter in series with each output phase [52]–[54].

The power circuit is illustrated in Fig.2.13 with only the H bridge of phase *a* shown in detail. As shown the DC source for the NPC inverter is provided by two series connected diode bridge rectifiers arranged in a 12-pulse configuration.

The H bridge DC links are not connected to an external DC power supply but they consist only of floating capacitors kept at a constant voltage by the control strategy. In this hybrid topology the NPC inverter provides the total active power flow. For a high-power medium-voltage NPC, there are advantages to using latching devices, such as integrated gate-commutated thyristors (IGCTs), rather than insulated-gate bipolar transistors (IGBTs) due to their lower losses and higher voltage blocking capability [52], [54], [55] imposing a restriction on the switching frequency. In contrast the H bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. This calls for the use of the IGBT.

The first interpretation is as a single hybrid multilevel inverter with a nine-level phase voltage, achieved by the cascade connection of a three-level NPC leg and an HB per phase. The second interpretation is as an NPC inverter with a series active filter that compensates for the harmonic content introduced by the low switching NPC stage. If the NPC bridge is to be modulated at a low switching frequency the second interpretation would seem to be more appropriate in devising a control algorithm, leading to the following two design challenges: 1) To determine the lowest value of the HB DC-link voltage V_{dc} that achieves adequate voltage harmonic compensation. 2) To devise a control algorithm that ensures that the floating DC links are properly regulated at this value.

2.7.7 HYBRID MULTILEVEL INVERTER BASED ON MAIN INVERTER AND CONDITIONING INVERTER

With minor changes in hybrid medium-voltage inverter based on a NPC inverter, hybrid multilevel inverter based on main inverter and conditioning inverter is obtained. Modifications done are shown in Fig. 2.14 the conditioning inverter is supplied by ultra capacitors as the DC source. The main and the conditioning inverters are in series. The output voltage of the main inverter is denoted v_1 and the output voltage of the conditioning inverter is denoted v_2 so the output voltage of the hybrid multilevel inverter is $v_o = v_1+v_2$

To explain the analysis of this circuit only one H bridge power cell is considered in each phase which means N=1 in Fig. 2.14, so the main inverter can be considered as a 3- level inverter. Its output voltage v_1 can be $+V_{dc}$, 0 and $-V_{dc}$.

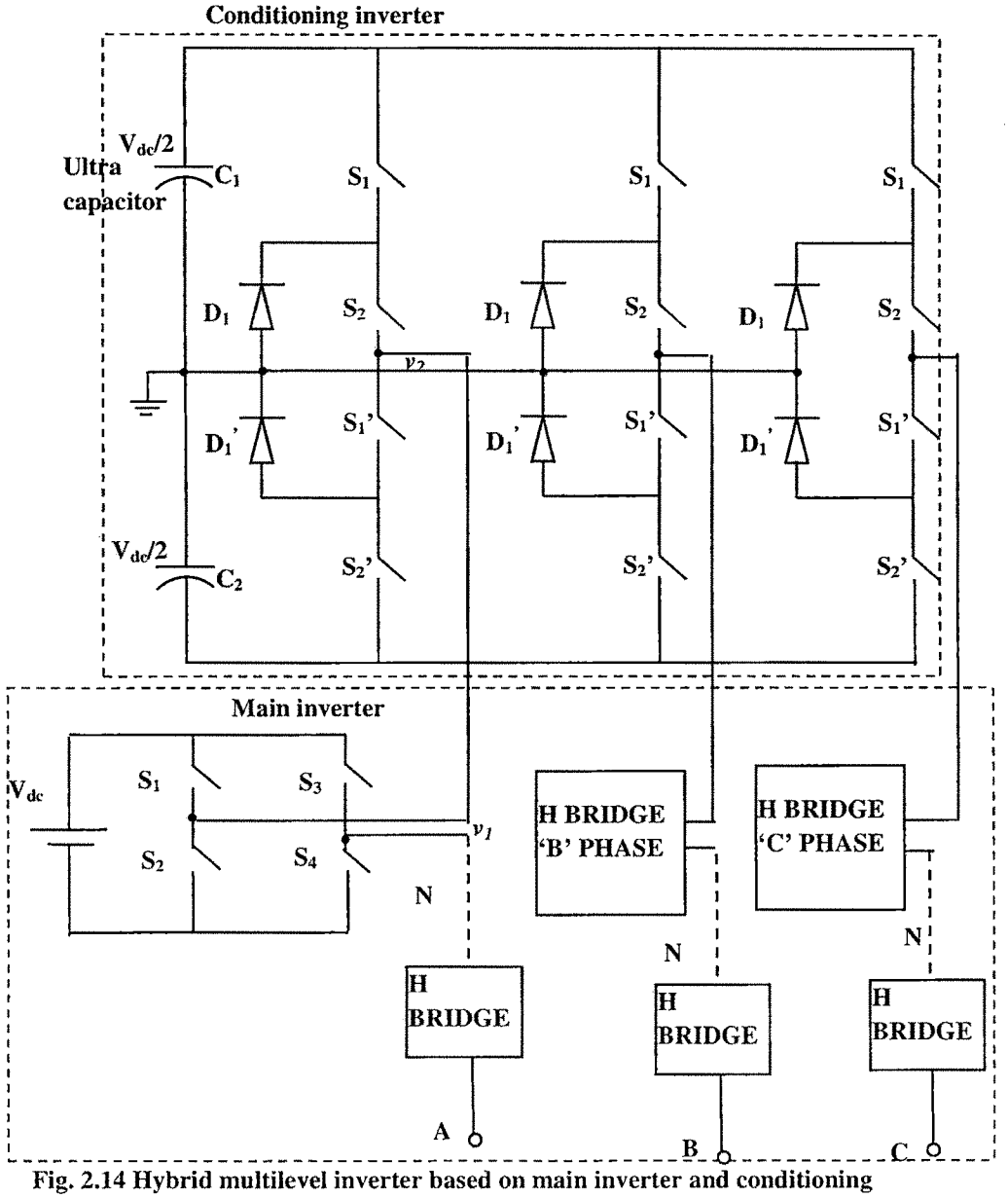


Fig. 2.14 Hybrid multilevel inverter based on main inverter and conditioning inverter

For the NPC conditioning inverter two ultra capacitors are in series and connected to the DC-link. If the DC voltage is considered as V_{dc}, and the two ultra capacitors are the same i.e.V_1= -V_2= $V_{dc}/2$. So the conditioning inverter output voltage v_c can be + $V_{dc}/2$, 0 and -$V_{dc}/2$. Therefore the inverter output voltage v_o can be -(V_{dc}+$V_{dc}/2$), -V_{dc},-(V_{dc}-$V_{dc}/2$), -$V_{dc}/2$, 0, $V_{dc}/2$, (V_{dc}-$V_{dc}/2$), V_{dc} and (V_{dc}+ $V_{dc}/2$) 9 possible output levels. When the ratio of V_{dc}:$V_{dc}/2$=1, the inverter can output 5 voltage

levels. When V_{dc} : $V_{dc}/2=3$, the inverter can output 9 voltage levels, which is called the maximal distension in the reference [56],[57].

This hybrid inverter is based on the traditional H-bridge topology incorporated with the conditioning inverter, thus some advantages can be obtained: 1) The conditioning inverter can be used as an energy storage device, which can store and reuse the braking energy of the motor. As a result, it improves the inverter efficiency. 2) The three-level NPC inverter can generate three different voltages, as the H-bridge cells do. So one H-bridge cell of each phase can be reduced by the conditioning inverter. This leads to a simplification of the feeding transformer. 3) The conditioning inverter can be considered as a SVC, which can deliver reactive power and improve the power factors of the system. 4) The conditioning inverter can be used to redundantly provide instantaneous energy when the main inverter cell is broken.

2.7.8 NEW HYBRID ASYMMETRICAL MULTILEVEL H-BRIDGE INVERTER

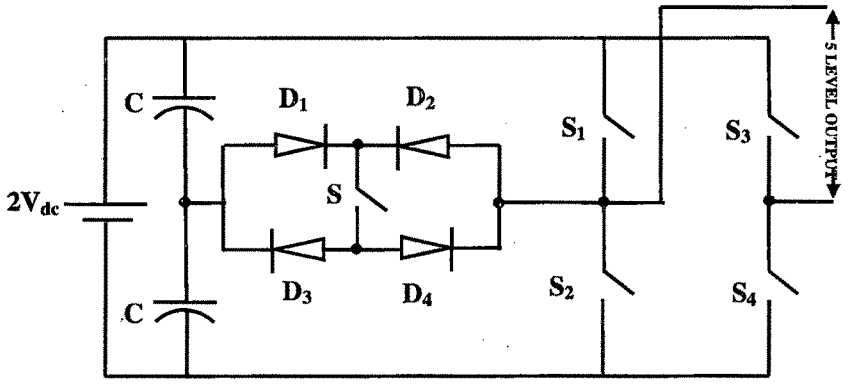


Fig. 2.15 New hybrid asymmetrical H-bridge multilevel inverter

Following the principle of increasing the number of output waveform voltage levels with less switching devices inverter topology is shown in Fig. 2.15. The new H-bridge topology with an auxiliary bidirectional switch can output maximum five level voltage waveform ($2V_{dc}$, V_{dc}, 0, $-2V_{dc}$, $2V_{dc}$). The switching combinations required to generate the five-level output waveform is as given in Table 2.8. In this configuration the two capacitors in the capacitive voltage divider are connected directly across the DC bus and since all switching combinations are activated in an output cycle the dynamic voltage balance between the two capacitors is automatically restored[55,58].

Table 2.8 Switching combinations for five level output voltage

S	S_1	S_2	S_3	S_4	Output Voltage
OFF	ON	OFF	OFF	ON	2 V_{dc}
ON	OFF	OFF	OFF	ON	V_{dc}
OFF	OFF	ON	OFF	ON	0
ON	OFF	OFF	ON	OFF	- V_{dc}
OFF	OFF	OFF	ON	OFF	-2 V_{dc}

2.7.9 HYBRID MULTILEVEL INVERTER WITH SINGLE DC SOURCE

This inverter includes a standard full bridge 3-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg as shown in Fig. 2.16.

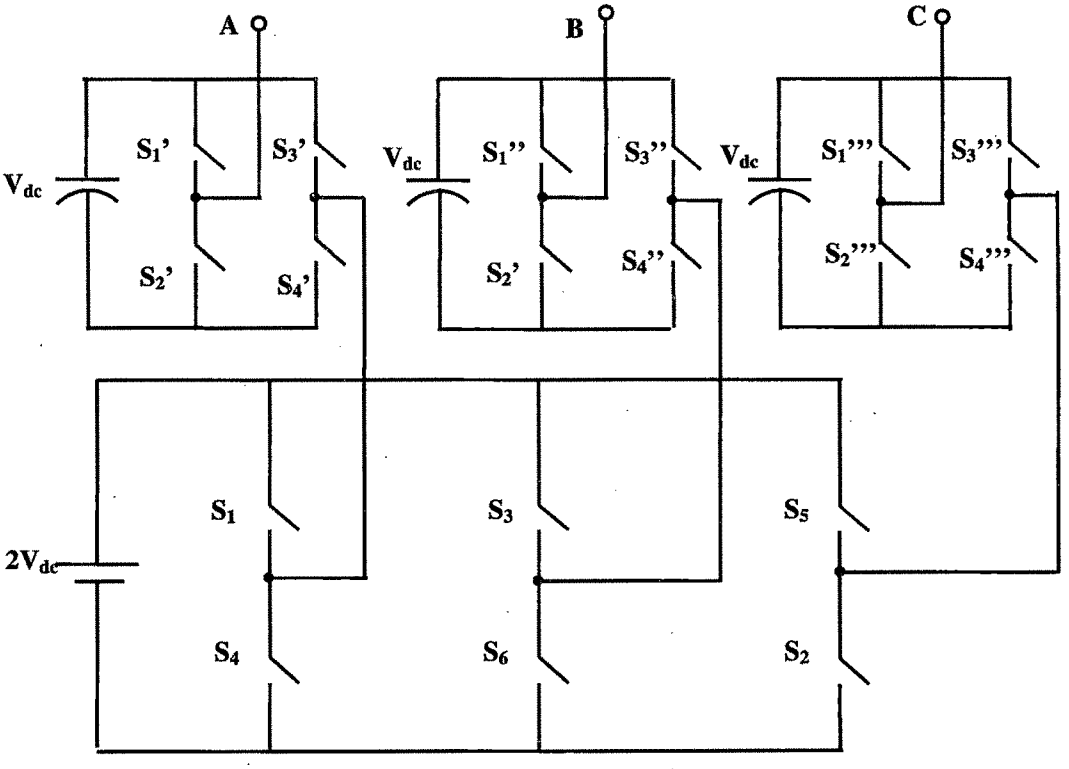


Fig. 2.16 Three phase hybrid multilevel inverter with single DC source

It uses only a single DC power source to supply a standard 3-leg inverter along with three full H-bridges supplied by capacitors or batteries. Traditionally, each H-bridge requires a DC power source [11,12,59-63]. The inverter can be used in electric vehicles (EV) / hybrid electric vehicles (HEV) to drive electric motor. And it can be applied for utility interface. As shown in Fig. 2.17 the output voltage v_1 of single leg (with respect to the ground) is either $+V_{dc}$ (S_5 closed) or $-V_{dc}$ (S_6 closed). This leg is connected in series

with a full H-bridge which in turn is supplied by a capacitor voltage. If the capacitor is used and kept charged to V_{dc}, then the output voltage of the H-bridge can take on the values + V_{dc} (S_1, S_4 closed), 0 (S_1, S_2 closed or S_3, S_4 closed), or – V_{dc} (S_2, S_3 closed).

Fig. 2.18 shows an output voltage example. The capacitor's voltage regulation control method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, S5 are closed depending on whether it is necessary to charge or discharge the capacitor. This method depends on the voltage and current not being in phase. That means one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current [64-68].

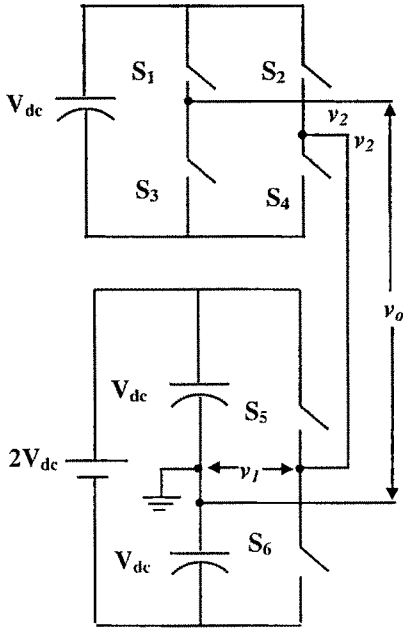


Fig. 2.17 Single phase hybrid multilevel inverter with single DC source

When the output voltage $v = v_1+v_2$ is required to be zero, one can either set v_1= + V_{dc} and v_2 = – V_{dc} or v_1 = + V_{dc} and v_2 = + V_{dc}. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage. During $\theta 1 \leq \theta \leq \pi$, the output voltage in Fig. 2.19 is zero and the current i > 0. If S_1 and S_4 are closed (so that v_2 = + V_{dc}) along with S_6 closed (so that v_1 = – V_{dc}), then the capacitor is *discharging* (ic = –i < 0 see Fig. 2.18) and $v = v_1+v_2 = 0$. On the other hand, if S_2 and S_3

are closed (so that $v_2 = -V_{dc}$) and S_5 is also closed (so that $v_1 = +V_{dc}$), then the capacitor is *charging* (ic = i > 0 see Fig. 2.18) and $v = v_1+v_2 = 0$. The case i < 0 is accomplished by simply reversing the switch positions of i > 0 case for charge and discharge of the capacitor.

As Fig. 2.19 illustrates, this method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the power factor. Thus by maintaining the regulation of the capacitor voltage simultaneously achieves an output voltage waveform which is 25% higher than that obtained using a standard 3-leg inverter by itself.

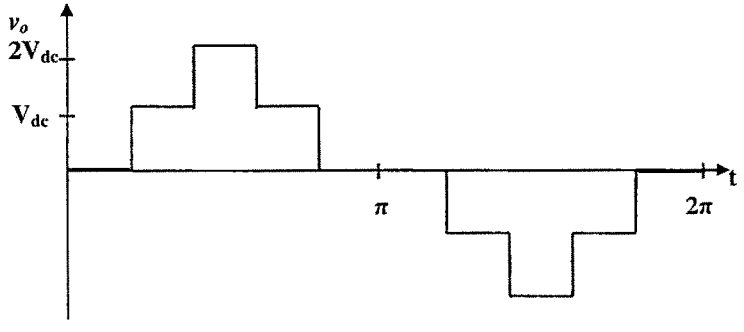


Fig. 2.18 Output voltage for single phase hybrid multilevel inverter with single DC source

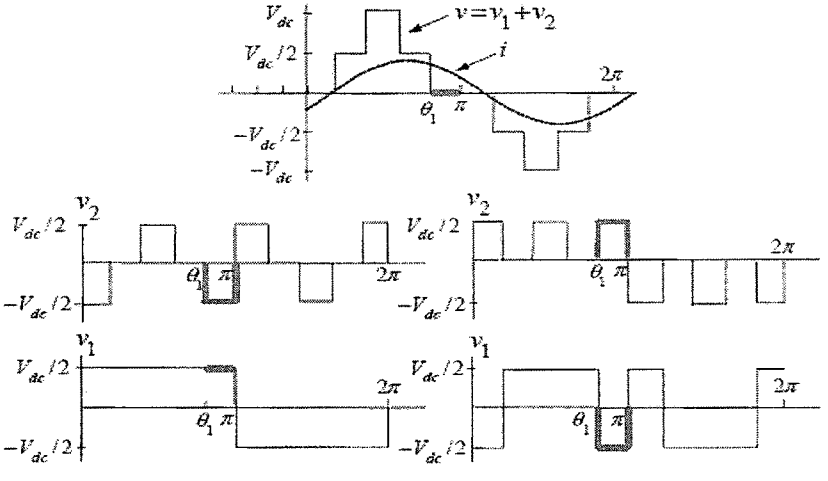


Fig. 2.19 Capacitor voltage regulation

2.8 SUMMARY

Thus comparative study for different multilevel inverters carried out in this research work is described and discussed. It can be concluded that every topology has its own advantages and disadvantages. Thus as per the application topology can be chosen and implemented. As asymmetrical multilevel inverters are alternative to minimize the harmonic distortion of the output voltages without increasing the number of power devices. The use of different DC voltage values naturally leads to hybrid multilevel topologies, which employ distinct types of semiconductors and modulation strategies, in an effort to optimize the power processing of the overall system. On the other hand, these features increase significantly the flexibility and complexity of hybrid multilevel inverter design. Distinct series connected cells hybrid multilevel inverter reduces the complexity for hybrid topology for distinct applications thus minimizing the number of switching devices and reducing the circulating energy among the series-connected cells. Compared with an H-bridge cascaded multilevel inverter, the number of overall insulated DC sources is reduced in the single phase hybrid symmetrical multilevel inverter while the number of semiconductors is kept the same. Thus, this concept appears as a useful and suitable solution for medium voltage applications where input-side insulation is required along with high efficiency and modularity. Furthermore, by reducing the number of insulated DC supplies, the number of cables connecting the input transformer terminals to the rectifying bridges is reduced.

New hybrid asymmetrical multilevel H-bridge inverter reduces the harmonic components of output voltage. Hybrid multilevel inverter based on main inverter and conditioning inverter topology is very suitable for the applications which need motors accelerating and braking frequently. The braking energy can be stored in the floating ultra capacitors of conditioning inverter to improve the efficiency and performance of the system. Hybrid multilevel inverter employing half-bridge modules and a three-phase inverter is able to provide better losses distribution among the power semiconductors and to limit the maximum device loss to a lower level when compared to a fully high frequency switched inverter. In this case devices are replaced with lower speed and lower forward voltage drop IGBTs for the four-level hybrid inverter which is able to achieve higher efficiency figures. In hybrid multilevel inverter with single DC source topology capacitor voltage balancing is of importance. This topology is generally used for HEV and EV applications, while hybrid clamped multilevel inverter reduces filter size.