CHAPTER 3

NOVEL MODULATION TECHNIQUES for MULTILEVEL INVERTER
and
HYBRID MULTILEVEL INVERTER

In different hybrid multilevel inverter topologies various modulation techniques can be applied. Every modulation technique has its own advantages and disadvantages. Depending on modulation index with respect to amplitude and frequency different modulation techniques can be studied.[1,2]

3.1 CLASSIFICATION OF DIFFERENT MODULATION TECHNIQUES

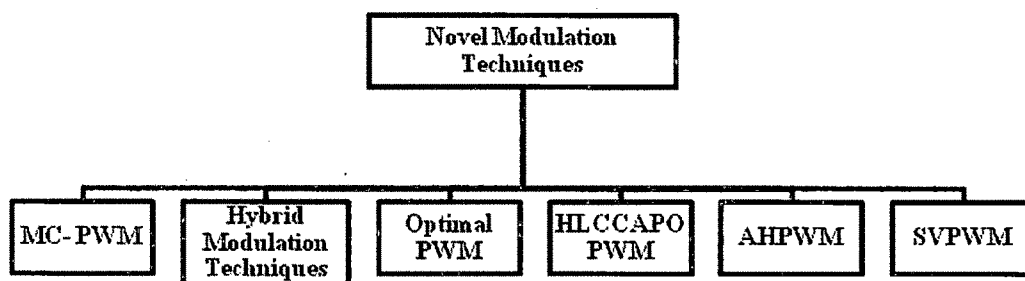Various modulation techniques are as shown in block diagram:

Fig. 3.1 Block diagram for novel modulation techniques

1. Multi carrier Pulse Width Modulation (MC-PWM).

2. Hybrid modulation techniques.

3. Synchronous pulse width modulation and higher frequency sub harmonic PWM

4. Higher and Lower Carrier Cells and Alternative Phase Opposition PWM (HLCCAPOPWM)

5. Alternative hybrid PWM (AHPWM).

6. Space vector PWM (SVPWM).

These modulation techniques can also be applied for other multilevel inverter configurations like diode clamped MLI, flying capacitor MLI and cascaded MLI. These modulation techniques are explained in general. Some modulation techniques are easily applicable to particular MLI but have to be modified for some other configurations. Modulation ratio plays an important role in all the techniques. Modulation can be over modulation or under modulation depending on modulation ratio and accordingly total harmonic distortion (THD) varies. While describing modulation techniques MLI topology, modulation ratio and THD are considered as major factors.

Following definitions are to be considered for further description:

- Amplitude Modulation ratio (m_a), defined as $m_a = A_m/A_c$, where A_m is the amplitude of the reference signal and Ac is the peak-to-peak amplitude of carrier signal. (For a N-level inverter, this ratio is defined as $m_a = A_m/(N-1)A_c$.

[1] Hina B. Chandwani and Meeta K. Matnani, "A review of modulation techniques for hybrid multilevel inverter" is presented in Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), December 2012 , pp. 1-7
[2] Hina B. Chandwani and Meeta K. Matnani , "A Review of Multicarrier Modulation Techniques for Various Hybrid Multilevel Inverter" International Journal of Engineering Associates, Volume 2 Issue 4, pp. 20-25   35

- Frequency modulation ratio (m_f), defined as $m_f = f_c/f_r$, where f_r is the reference signal frequency and f_c is the carrier signal frequency.

- β angle that the relative phase displacement between the carrier and the reference signal and in this analysis it is assumed to be zero.

3.2   MULTI CARRIER PULSE WIDTH MODULATION

The following section describes different multicarrier PWM techniques. The multicarrier PWM can be broadly classified as shown in Fig. 3.2.
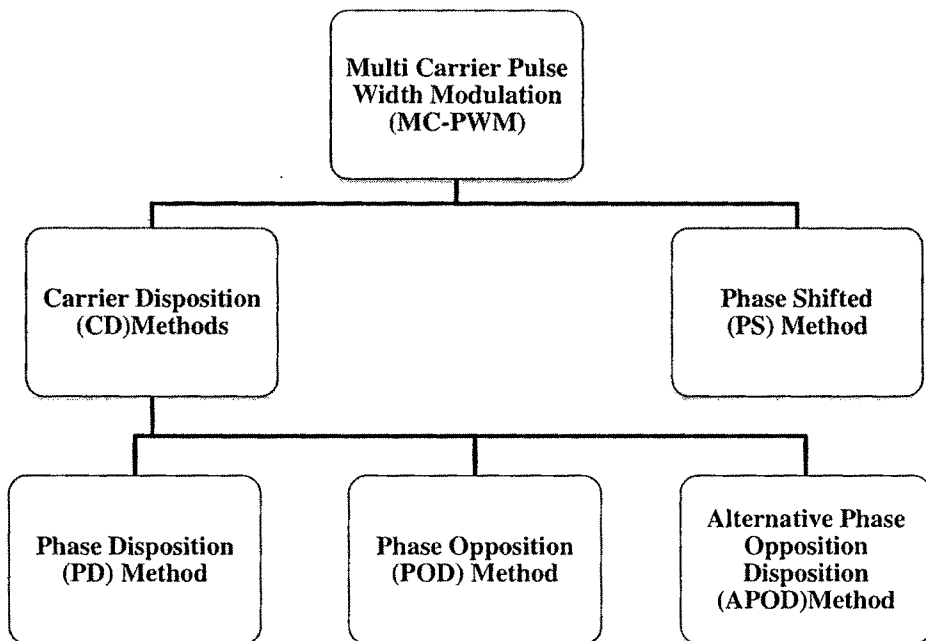

Fig. 3.2 Classification for multicarrier pulse width modulation

The multicarrier PWM technique uses several triangular carrier signals keeping only one modulating sinusoidal signal. For an n level inverter n-1 carriers are employed [1] – [2]. The carriers have the same frequency and same peak to peak amplitude but are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency 50 Hz. At every instant each carrier is compared with the modulating signal. Each comparison gives one if the modulating signal is greater than the triangular carrier, zero otherwise. The results are added to give the voltage level which is required at the output terminal of the inverter. Multicarrier PWM technique can be categorized into 2 groups. 1) Carrier disposition techniques (CD) where the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform

amplitude. 2) Phase shifted PWM technique, where the multiple carriers are phase shifted accordingly [3].

3.2.1 CARRIER DISPOSITION TECHNIQUES (CD)

This carrier disposition can be classified into the following three techniques i) phase disposition technique ii) phase opposition technique and iii) alternative phase opposition disposition technique. These techniques are usually applied to the neutral point clamped topology [4] - [7]. These techniques may not be used for the H-Bridge inverter applications directly. But by using discontinuous PWM reference signals with phase-shifted carrier strategy may be implemented to apply PD technique to the H-Bridge inverter [8].
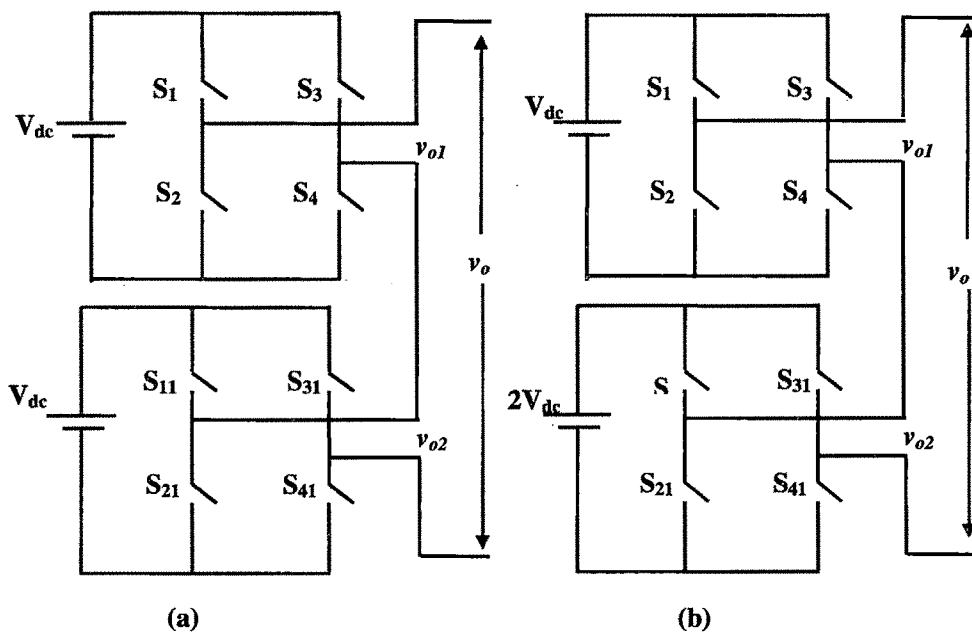

Fig. 3.3 Cascaded H-bridge inverter (a) symmetric five level (b)Asymmetric seven level

For description of the three modulation techniques mentioned a five level symmetric cascaded H-bridge inverter is considered as shown in Fig. 3.3(a). Also these modulation techniques can be applied to asymmetric multilevel inverter, diode clamped MLI, flying capacitor MLI and other hybrid MLI configurations.

3.2.2 PHASE DISPOSITION (PD) TECHNIQUE

The phase disposition technique has all carrier waveforms in phase with same frequency and amplitude, as shown in Fig. 3.4 (a). The zero reference is placed in the middle of the carrier sets. For this technique, significant harmonic energy is concentrated

at the carrier frequency [9]. The PD technique yields only odd harmonics for odd m_f and yields odd and even harmonics for even m_f (β =0) [10]. PD-PWM modulation can also be used in asymmetric multilevel topology [11] and as the number of voltage levels are increased the harmonic contents are decreased. Fig. 3.4 (b) shows output phase voltage for five level MLI using PD modulation technique.

For all simulation results on Y-axis voltage in volts is taken and on X-axis time is taken in seconds.
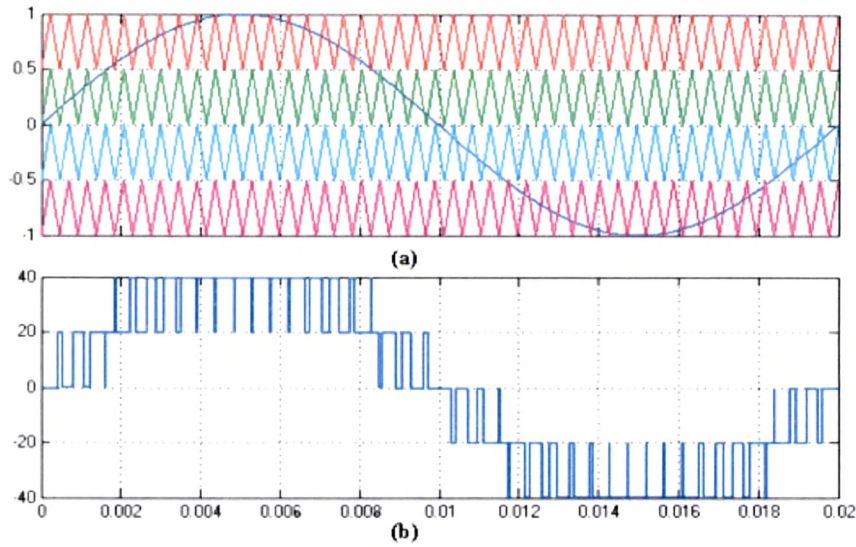
Fig. 3.4 (a) Phase Disposition technique (b) Five level inverter output voltage

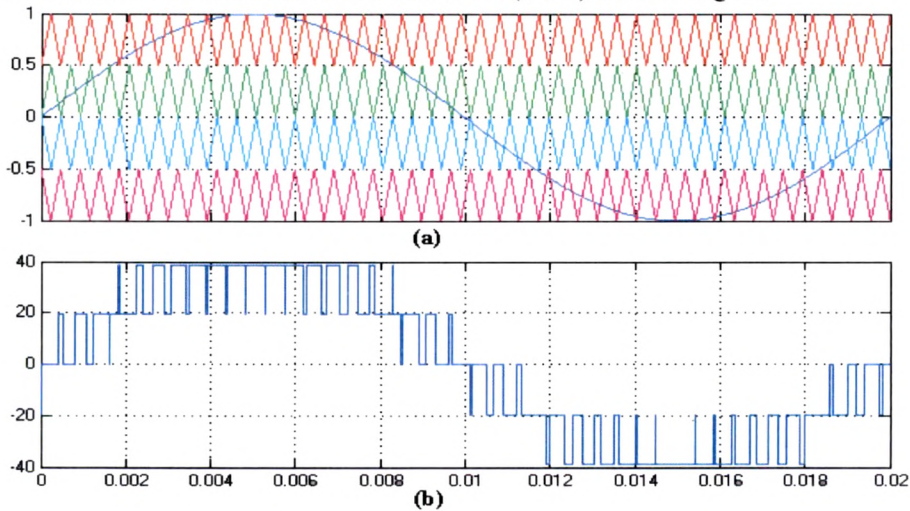### 3.2.3   PHASE OPPOSITION DISPOSITION (POD) TECHNIQUE

Fig. 3.5 (a) Phase Opposition Disposition technique (b) Five level inverter output voltage

With the POD technique the carrier waveforms above or below the zero reference value are in phase. However, they are phase shifted by 180° between the carrier waveforms above and below zero, as shown in Fig. 3.5 (a). The POD technique yields quarter wave symmetry for even m_f and odd symmetry for odd m_f. In this modulation, dominant harmonics are on the sideband of the first carrier ($m_f \pm 1$) and the phase voltage harmonic at the carrier frequency is not considerable [12]. POD modulation contains significant harmonics in the line voltage spectrum, especially in the first carrier band. Fig. 3.5 (b) shows output phase voltage for five level MLI using POD modulation technique.

3.2.4 ALTERNATIVE PHASE OPPOSITION DISPOSITION (APOD) TECHNIQUE

All carrier waveforms in this APOD technique are phase-displaced by 180° alternatively, as shown in Fig. 3.6 (a).
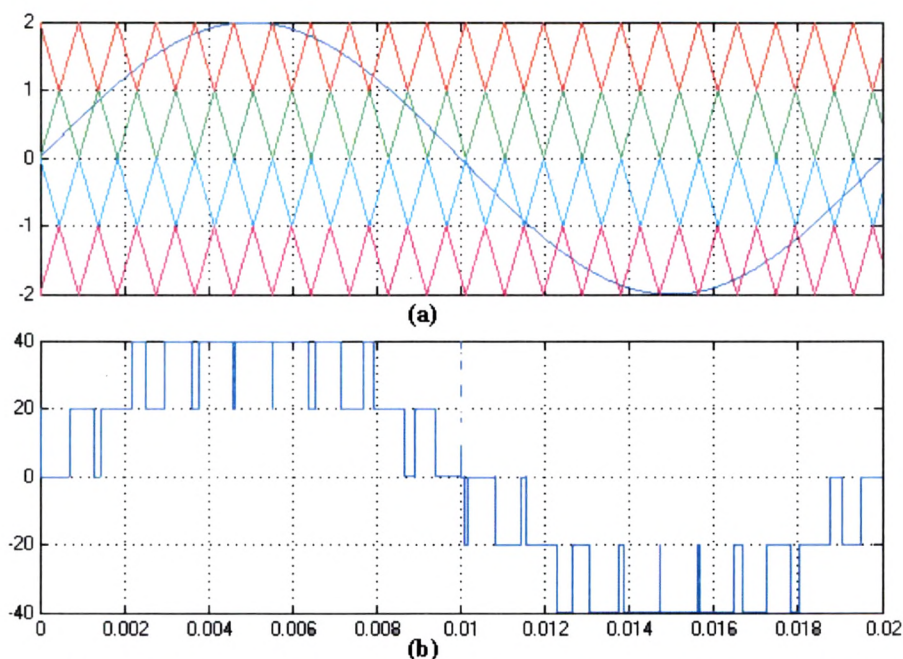

Fig.3.6 Alternative Phase Opposition Disposition technique (b) Five level inverter Output Voltage

This technique requires each of the four carrier waveforms, for a five level inverter output waveform, to be phase displaced from each other by 180° alternately. The voltage at the output of a five level inverter which uses APODPWM control technique is as the following:

- The inverter switches to V/2 if the reference signal is higher than all of carrier signals.

- The inverter switches to V/4 if the reference signal is lower than two above carrier signals and higher than two below carrier signals.

- The inverter switches to –V/4 if the reference signal is lower than two below carrier signals and higher than two above carrier signals.

- The inverter switches to –V/2 if the reference signal is lower than all of carrier signals

It can be seen that APOD modulation does not produce a first carrier harmonic. Instead the dominant harmonics are channeled into the sidebands around the first carrier harmonic. Therefore, since only the triple sidebands away from the carrier frequency cancel in a three phase system, APOD modulation contains some considerable harmonic energy in the line m_f is even. If m_f is odd, then the output waveform has odd symmetry. Fig. 3.6 (b) shows output phase voltage for five level MLI using APOD modulation technique.

3.2.5   PHASE SHIFTED (PS) TECHNIQUE

In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by $\Phi cr = 360°/(m – 1)$ where m is voltage level of multilevel inverter.
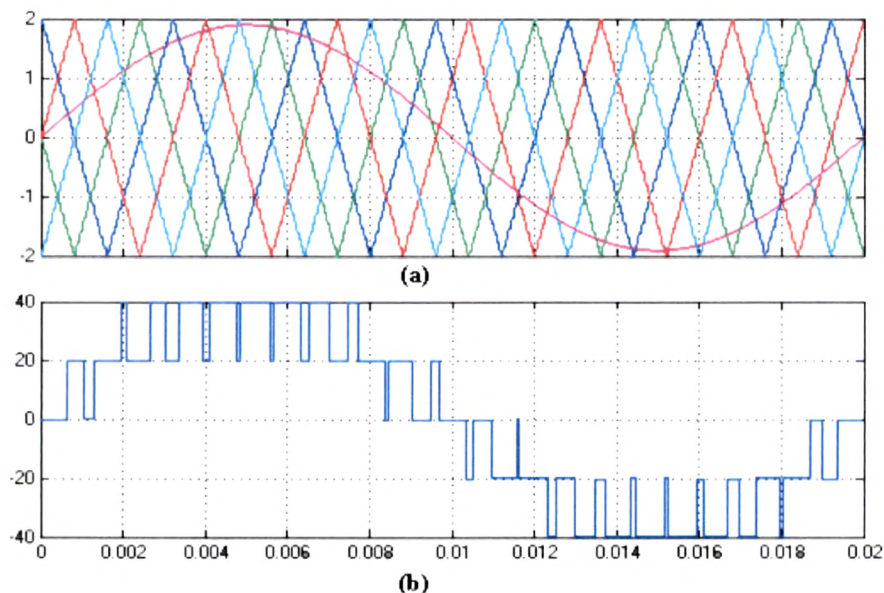

Fig.3.7 (a) Phase Shifted Technique (b) Five level inverter Output Voltage

In general, a multilevel inverter with m voltage levels requires (m – 1) triangular carriers. The gate signals are generated by comparing the modulating wave with the carrier waves. It means for the five level inverter, four triangular carriers are needed with a 90° phase displacement between any two adjacent carriers as shown in Fig. 3.7 (a) Fig. 3.7 (b) shows output voltage for five level MLI [13].

3.3   HYBRID MODULATION TECHNIQUES

Hybrid PWM (H-PWM) is an extension of PWM for CHB with unequal dc sources [14]. The hybrid PWM is the combination of low frequency PWM and high frequency SPWM. The main challenge is to reduce the switching losses of the inverter by reducing the switching frequency of the higher power cells. Therefore, instead of using high frequency carrier-based PWM techniques in all the cells, the high-power cells are operated with square waveform patterns, switched at low frequency, while only the low power cell is controlled with unipolar PWM. An optimized hybrid PDPWM technique commutates the power switches at high frequency and low frequency sequentially.

3.3.1   HYBRID MODULATION STRATEGY

A hybrid modulation strategy combines fundamental frequency switching for higher power cells and open loop PWM control for the low power cell switching at higher frequency [14]-[17]. Fig. 3.8 shows basic block diagram for such technique to be implemented. With this modulation technique the effective spectral response of the output depends on low power cell like IGBT switching while the overall voltage generation is decided by voltage ratings of higher power cells like GTO.

As shown in Fig. 3.8 the command signal is compared with a threshold voltage. If it is larger than the threshold then high voltage cell inverter contributes to the output. The difference between the output of the high voltage inverter and the command signal is then compared against a PWM (ramp) signal to modulate the low voltage cell inverter. The resultant phase voltage obtained is shown in Fig. 3.11. The switching patterns for the high voltage cell inverter and low voltage cell inverter are shown in Fig. 3.9 and 3.10. It may be seen that although the high voltage cell inverter switching is stepped (Fig. 3.9), the overall waveform quality is mainly decided by the intermediate low voltage cell inverter switching (Fig. 3.10). The high voltage cell inverter participates in synthesizing the required high voltage level while the low voltage cell inverter acts as a harmonic compensator.
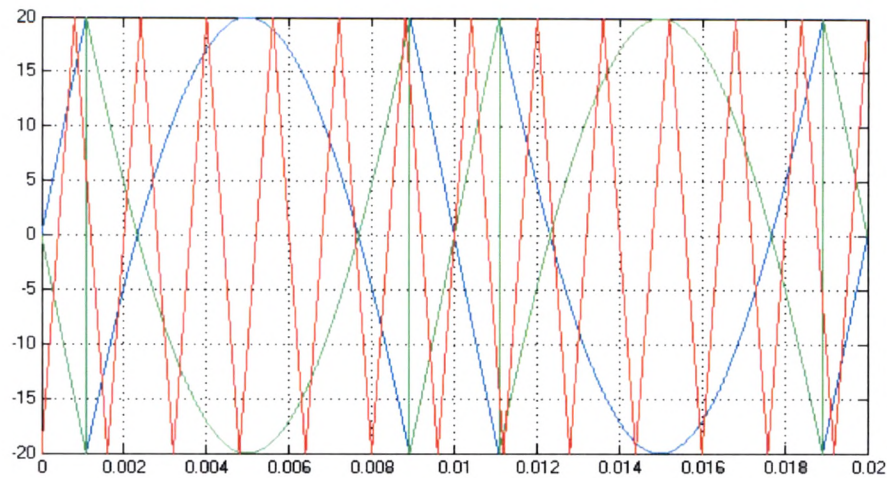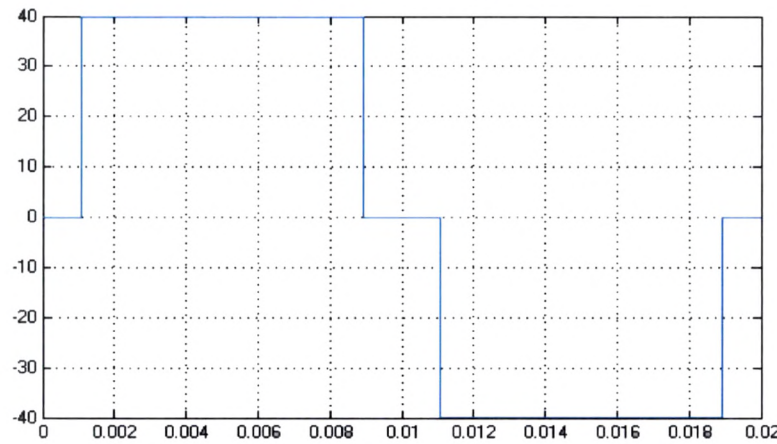
Fig. 3.8 Hybrid modulation strategy
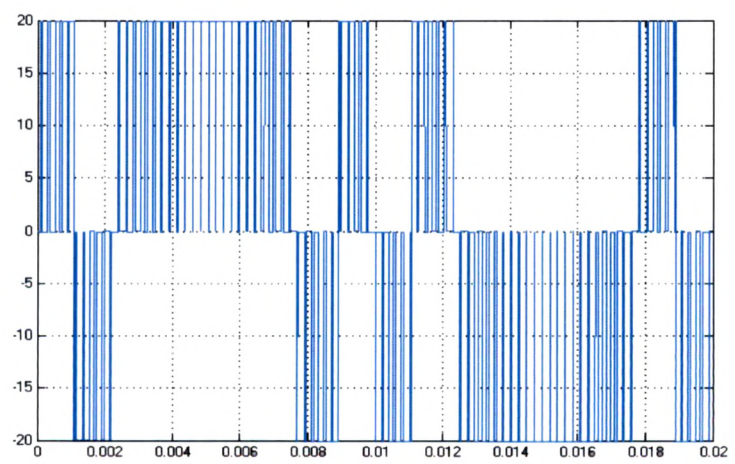

Fig. 3.9 High power cell switching

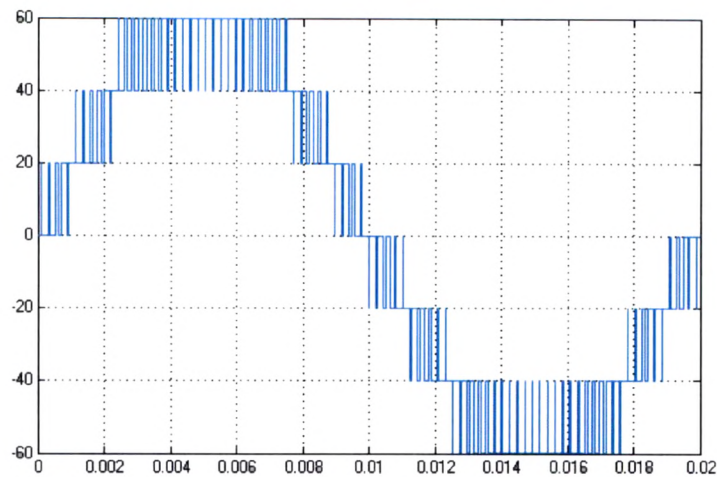**Fig. 3.10 Low power cell switching**

Fig. 3.11 Output phase voltage

3.3.2   INVERTED SINE CARRIER PWM (ISCPWM)

This control strategy replaces the conventional triangular based carrier waveform by inverted sine wave which has a better spectral quality and a higher fundamental output voltage without any pulse dropping [18]. This technique combines the advantage of inverted sine and constant or variable frequency carrier signals as shown in Fig. 3.12 and Fig. 3.13 respectively. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been shown [19]-[20]. Both the techniques are explained in brief.
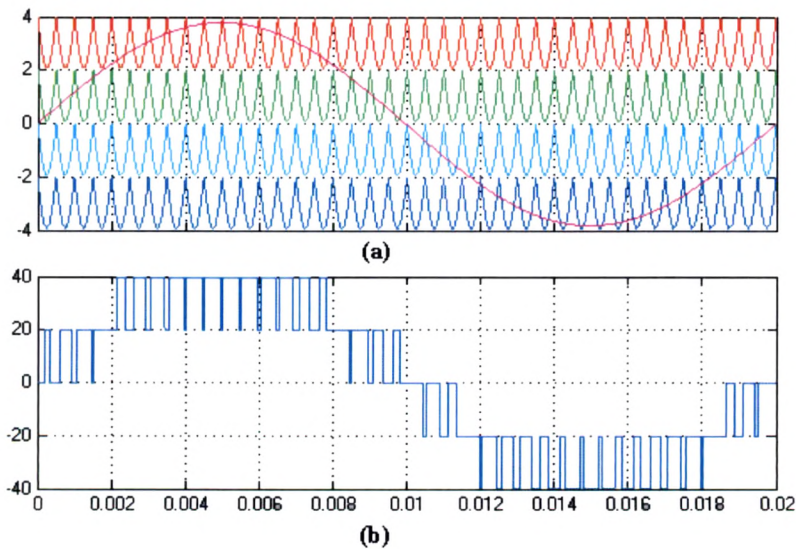

Fig. 3.12 (a) Inverted sine technique (b) Five level inverter output voltage

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Fig. 3.12 shows application of unipolar PWM to inverted sine carrier which results in the reduction of carrier frequencies or its multiples and significant reduction in switching losses. Thus advantage of inverted sine and unipolar PWM are combined to improve the performance of the hybrid multilevel inverter. The inverted sine carrier PWM (ISCPWM) technique uses the sine wave as reference signal while the carrier signal is an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. From the Fig. 3.18 it is clear that the pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.

3.3.3 VARIABLE FREQUENCY INVERTED SINE CARRIER PWM (VFISPWM)

The VFISPWM technique provides an enhanced fundamental voltage, lower THD and minimizes the switch utilization among the bridges in inverters [21]. The number of active switching among the bridges is balanced by varying the carrier frequency based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all bridges. Using the slope values of the carrier bands, the new frequencies are calculated. The number of switching actions is balanced for all the switches in bridge with low voltage level switches using the VFISPWM technique. The band dwell time of the modulating wave in each carrier and the frequency ratio (m_f) can be calculated.
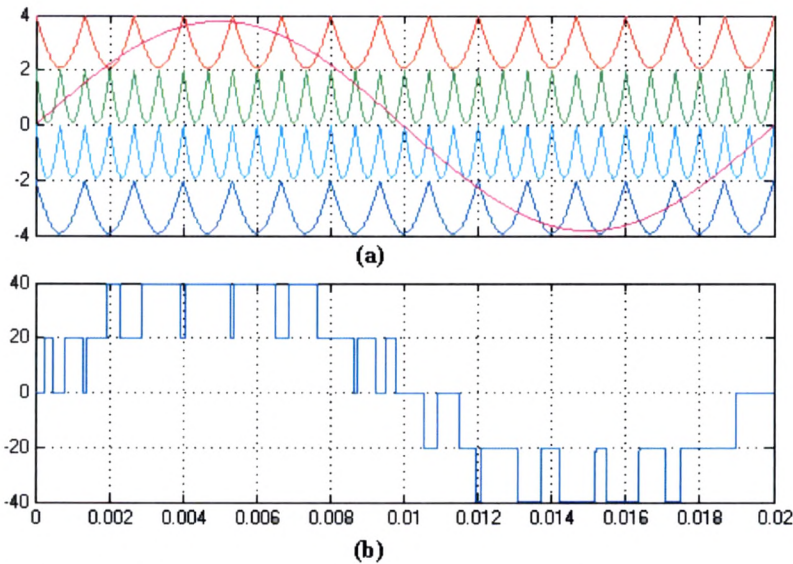

Fig. 3.13 (a)Variable Frequency Inverted Sine Carrier (b) Five level inverter output voltage

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As seen hybrid PWM is the combination of low frequency PWM and high frequency SPWM. In each cell of cascaded inverter, the four power devices are operated at two different frequencies, two being commutated at low frequency, i.e. the fundamental frequency of the output, while the other two power devices are pulse width modulated at high frequency. This arrangement causes the problem of differential switching losses among the switches.

An optimized sequential signal is added to the hybrid PWM pulses to overcome this problem. The low and high frequency PWM signal are shown in Fig. 3.14 (c.f [22]). An optimized hybrid PDPWM technique commutates the power switches at high frequency and low frequency sequentially.

A common sequential signal and low frequency PWM signals are used for all cells in cascaded inverter. A high frequency SPWM for each cell is obtained by the comparison of the rectified modulation waveform with corresponding phase disposition carrier signal. The low frequency PWM signal should be synchronized with the modulation waveform. In Fig. 3.15 (c.f [22]) the gate pulses are generated by a hybrid PWM controller. This controller is designed to mix the sequential signal low frequency PWM and high frequency phase disposition sinusoidal PWM and to generate the appropriate gate pulses for cascaded inverter.

3.3.4 OPTIMIZED HYBRID PDPWM

An optimized hybrid PDPWM switching pattern can be generalized for N level inverter. Let N be the number of levels of the cascaded inverter. M is the number of inverter cells, M=N-1/2. The modulation index is therefore defined as $mi= A_m /MA_c$ and the definition of the frequency ratio $mf= f_m/f_c$, where f_c as carrier frequency and f_m as modulating signal frequency. The modulating signal A_m is modified based on number of levels and modulation index. A modified sinusoidal modulating signal is then compared with each phase disposition carrier signal separately to generate M number of high frequency sinusoidal PWM signals. A hybrid PWM controller is used to mix low frequency PWM and the corresponding high frequency SPWM for M^{th} inverter cell. This hybrid PWM for M^{th} inverter cell is then optimized with sequential signal in order to equalize switching transitions. Similarly, hybrid PWM pulses are developed for all cells in any level cascaded inverter [22].
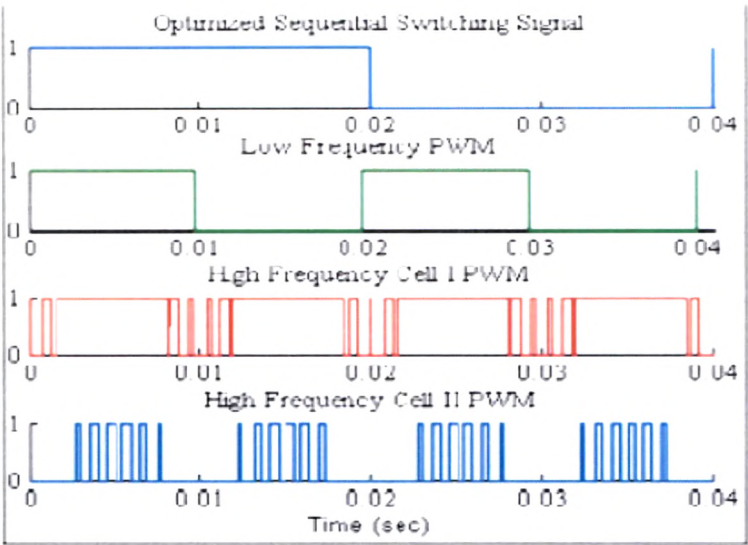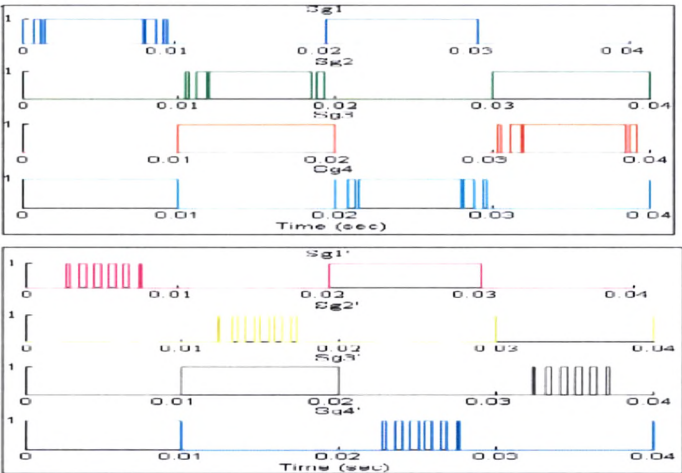
Fig. 3.14 Low and high frequency PDPWM

Fig. 3.15 Optimized hybrid PDPWM switching pattern for five level cascaded MLI

3.4   SWITCHING FREQUENCY OPTIMAL PWM

When the carrier wave is synchronized with the modulating wave (mf is an integer), the modulation scheme is known as synchronous PWM. The synchronous PWM scheme is more suitable for implementation with a digital processor. For a m-level inverter, m-1 carriers with the same frequency fc and the same amplitude Ac are disposed such that the bands they occupy are contiguous [28]. The reference wave form has peak to peak amplitude Am, the frequency fm, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If

the reference is greater than s carrier signal, then they active device corresponding to that carrier is switched off. This technique is further explained in following section.

3.4.1 MULTI CARRIER SWITCHING FREQUENCY OPTIMAL PWM (MC-SFO PWM)

The other technique to improve the gain of pulse width modulator in a multilevel inverter is Switching Frequency Optimal PWM (SFO-PWM) [23]. This modulation is similar to the group of pure sinusoidal PWM (SPWM) and applicable for three-phase systems but the zero sequence (3rd harmonic) of voltage is injected to each reference signals [24]. This technique calculates the average value of maximum and minimum of instantaneous reference voltages and for all the modulation waveforms subtract this value from the reference voltage.

$$V_{offset} = Max(V_a, V_b, V_c) + Min(V_a, V_b, V_c)$$

$$V\_aSFO = V\_a - V\_offset$$

$$V\_bSFO = V\_b - V\_offset$$

$$V\_cSFO = V\_c - V\_offset$$

Analog circuit to make the reference signal of SFO-PWM is shown in Fig. 3.16 [25] – [27]. Fig. 3.17 shows the SFO-PWM with injection of a third-harmonic into the reference waveforms which achieves a 15% increase in modulation index over sinusoidal PWM before over modulation nonlinearities occur. It is simply because of the reduced height of the three phase reference envelope that is achieved by third-harmonic injection. In this technique, the 3rd harmonic is cleared in three-phase system.

The results indicate that the third-harmonic injection offers minimal harmonic advantage for PWM of multilevel inverters, since the harmonic distribution of line voltage spectrum is not improved significantly. Therefore, this optimization only has the value to increase the available linear modulation region if this is required [36].
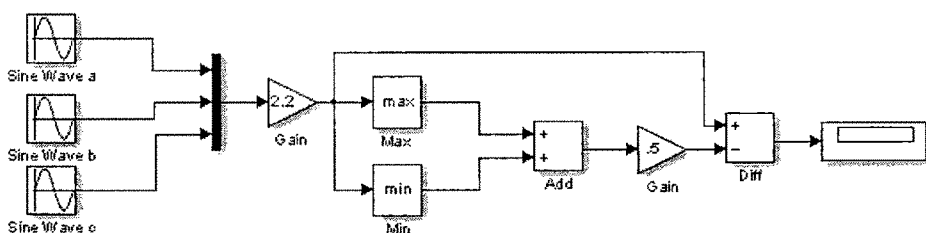

Fig. 3.16 Analog circuit to make the reference signals in SFO-PWM technique
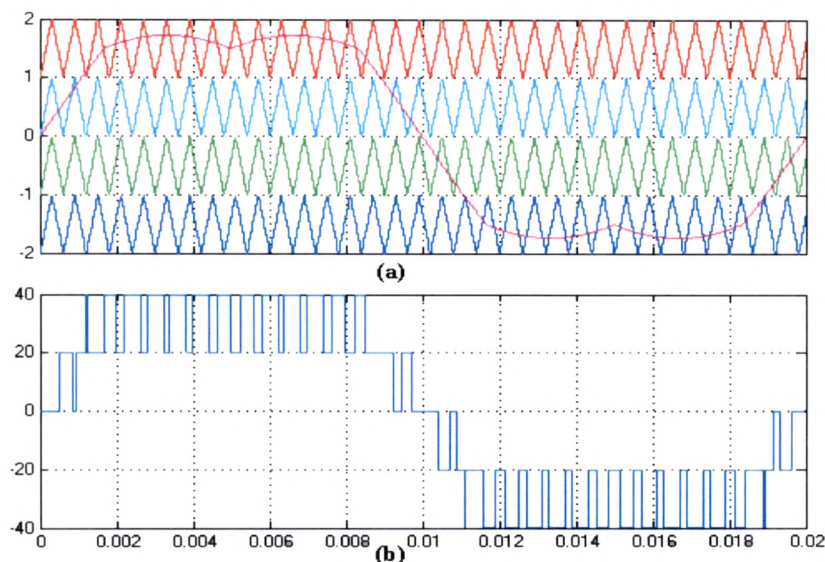
Fig. 3.17 SFO-PWM technique for a 9-level asymmetric inverter output

3.4.2   PHASE SHIFTED CARRIER SWITCHING FREQUENCY OPTIMAL PULSE WIDTH MODULATION (PSC-SFO PWM) OR PHASE-SHIFTED SUBOPTIMAL CARRIER PWM (PS-SUB-PWM)

Fig.3.18 shows the phase shifted carrier SFO PWM modulating signal generation [28]. The technique takes the instantaneous average of the maximum and minimum of the three reference voltages (Va, Vb, Vc) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms, which is shown in Fig.3.19. From the above criteria the following equation are obtained.

$$Vcarrier = \{max\ (Va,Vb,Vc\ ) + min\ (Va,Vb,Vc\ )\} / 2$$

$$VaSFO = Va - Vcarrier$$

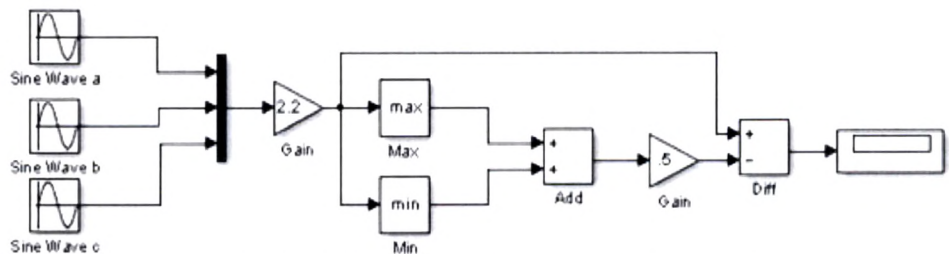$$VbSFO = Vb - Vcarrier$$

$$VcSFO = Vc - Vcarrier$$

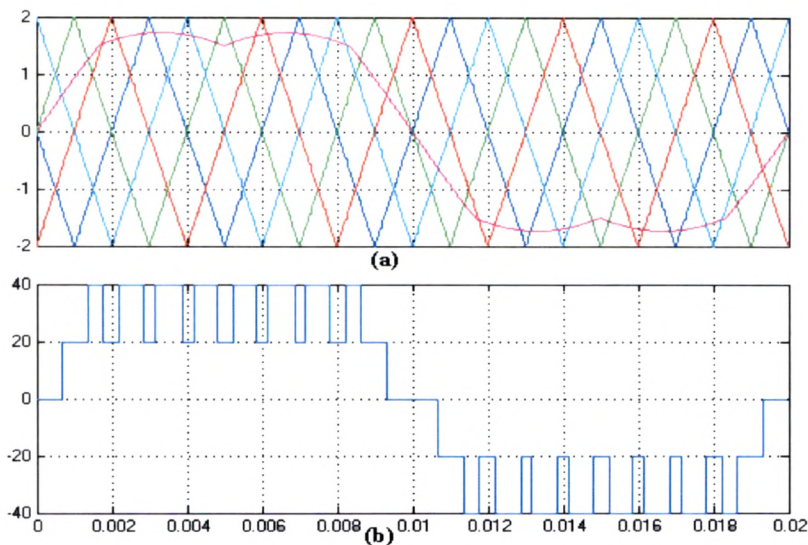**Fig.3.18 PSC-SFO PWM modulating signal generation**

Fig. 3.19 Phase shifted carrier switching frequency optimal pulse width modulation

The carrier voltage is the average of maximum and minimum value of Va,Vb,Vc. The phase voltage using SFO is the difference between reference voltages to carrier voltage. The zero sequence modification made by the SFO PWM technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs.

Fig. 3.19 shows an example of the five-level PS-SUB-PWM technique where switching angles in 1/4-period are defined.

3.5 HIGHER AND LOWER CARRIER CELLS AND ALTERNATIVE PHASE OPPOSITION PW (HLCCAPOPWM)

The PWM control technique based on the improvement of carrier phase disposition PWM (PDPWM) is called higher and lower carrier cells alternative phase opposition PWM (HLCCAPOPWM) for the hybrid-clamped multilevel inverter Fig. 3.20 [30].
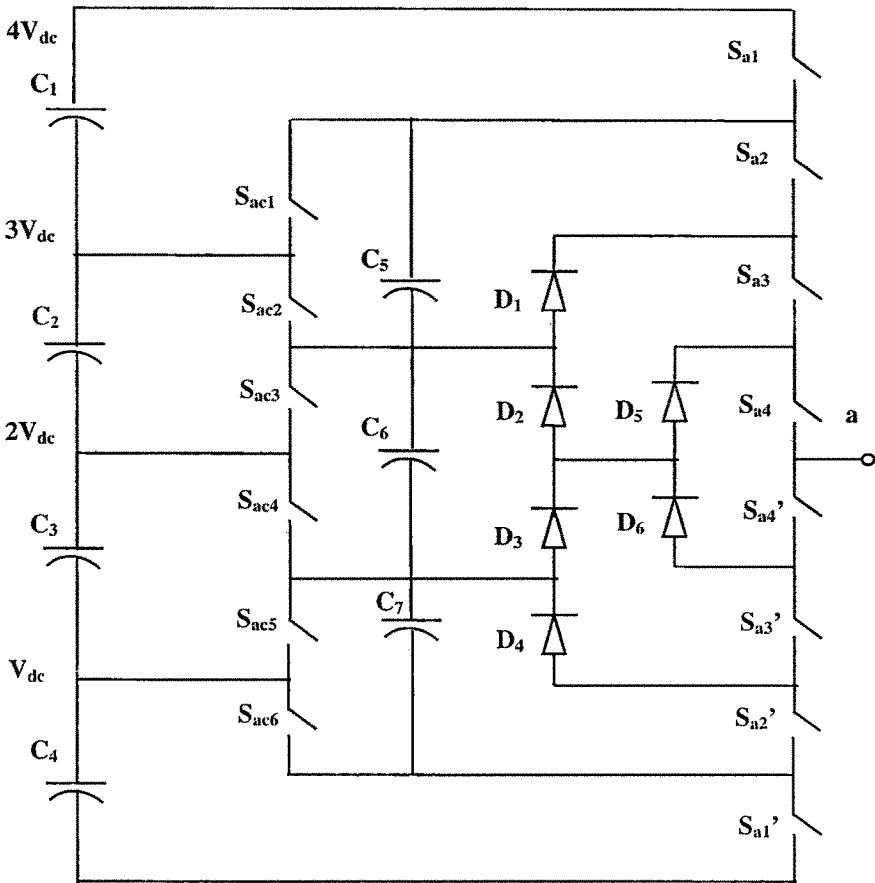
Fig. 3.20 Hybrid clamped five level inverter

3.5.1 PRINCIPLE OF HLCCAPOPWM

The principle of the HLCCAPOPWM technique is explained by introducing the concept of carrier cell. When the carrier waveforms are divided according to the carrier period then the individual triangle wave is called carrier cell as shown in Fig. 3.21[30]..

This technique can reduce switching losses and improve the output harmonic performance in low harmonic bands. The concept of carrier cell provides a new clue for improving carrier waveforms of switching devices for the hybrid-clamped multilevel inverter. The novel PWM technique can effectively reduce the number of device switching on or off in different degrees hence reducing switching losses within broad modulation index range. In other words the switching frequency with the HLCCAPOPWM technique can be increased under the condition of the same switching losses with the PDPWM technique and then the harmonic content of output voltage will

be further lowered. In addition the energy of lower harmonics transfers to higher harmonics band with the HLCCAPOPWM technique. The reduction of the energy of lower harmonics can simplify the design of output filter and reduce its size.
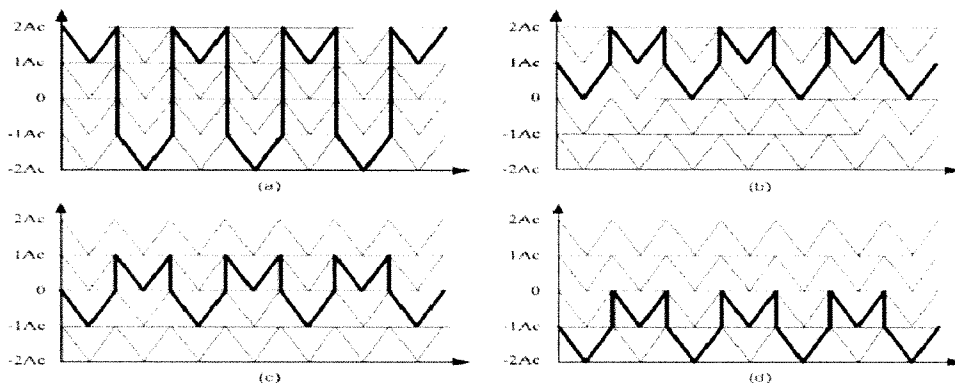

Fig. 3.21 Carrier waveforms of the upper four main switching devices for a hybrid-clamped five-level inverter with the PDPWM technique. (a) Carrier of S_{a1}. (b) Carrier of S_{a2}. (c) Carrier of S_{a3}. (d) Carrier of S_{a4}

3.5.2   HLCCAPOPWM CONTROL TECHNIQUE

Using the concept of carrier cell, it can be seen from Fig. 3.21 that the carrier waveforms of the PDPWM technique for hybrid-clamped multilevel inverters have two features: 1) all the carrier cells are in phase and 2) the carrier cells of main switching devices S_{a1}, S_{a2}, S_{a3}, and S_{a4} are positioned on the higher and lower carrier bands respectively. Furthermore the higher and the lower carrier cells alternate by turns constantly [31]. For S_{a1} the higher carrier cells are positioned on the first carrier band and the lower ones on the fourth carrier band. For S_{a2} the higher carrier cells are positioned on the first carrier band and the lower ones on the second carrier band. For S_{a3} the higher carrier cells are positioned on the second carrier band and the lower ones on the third carrier band. For S_{a4} the higher carrier cells are positioned on the third carrier band and the lower ones on the fourth carrier band. If the higher carrier cells and the lower ones are in phase the corresponding PWM pulse waveform is shown in Fig. 3.22(a) [31] which is produced by a higher carrier cell intersecting the modulation wave. As it is known the device controlled by this PWM pulse waveform will turn on or off four times. If the higher carrier cells are reversed then the higher carrier cells and the lower ones are in phase opposition. In addition the corresponding PWM pulse waveform is shown in Fig. 3.22 (b) c.f [31] which is also produced by a higher carrier cell intersecting the same modulation wave. It is clear that the number of device switching on or off is two, only

half of that shown in Fig. 3.22 (a). Fig. 3.23 c.f [31] shows two PWM pulse waveforms respectively produced by two kinds of carrier cells in phase opposition intersecting a certain modulation waveform.
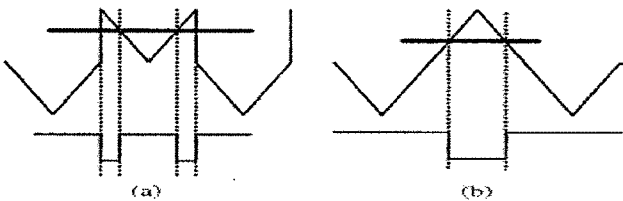

Fig. 3.22 Device switching on or off (a) Higher carrier cells and lower carrier cells in phase. (b) Higher carrier cells and lower carrier cells in phase opposition
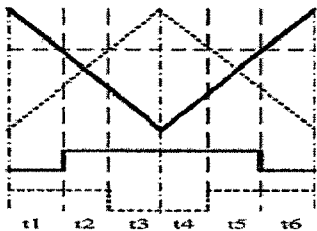

Fig. 3.23 PWM pulse waveforms respectively produced by the carrier cells in phase opposition intersecting a certain modulation wave
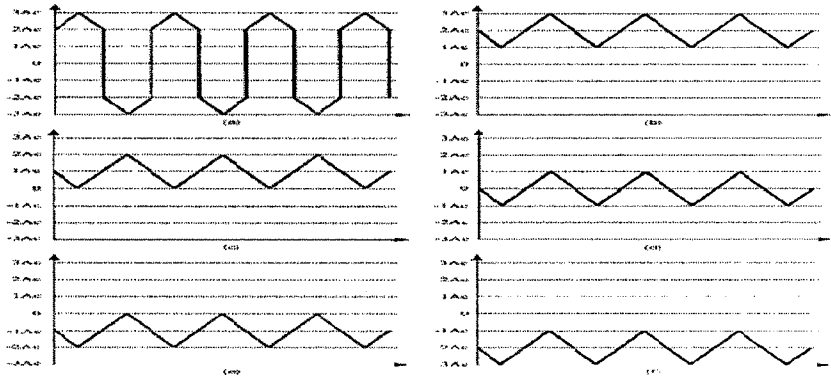
Fig. 3.24 Carrier waveforms of the upper six main switching devices for a seven level inverter with the HLCCAPOPWM technique. (a) Carrier of S_{a1}. (b) Carrier of S_{a2}. (c) Carrier of S_{a3}. (d) Carrier of S_{a4}. (e) Carrier of S_{a5}. (f) Carrier of S_{a6}

If the duty cycles during one carrier period of two PWM pulses are equal then the instantaneous values of the output voltage fundamental component are also equal so the modulation performance of two kinds of carrier cells in phase opposition as shown in Fig. 3.23 are identical. Therefore it is feasible to improve the carrier waveforms of every switching device shown in Fig. 3.21 by reversing all the higher carrier cells to reduce the

number of device switching on or off. As a result the higher and lower carrier cells will be in phase opposition for every switching device. The improved carrier waveforms for switching devices S_{a1}, S_{a2}, S_{a3}, and S_{a4} are shown in Fig. 3.24 c.f [31].

3.6   ALTERNATIVE HYBRID PWM (AHPWM)

Fig. 3.25 [32] shows the carriers of another PDPWM technique. The initial phase angle of the triangle carrier waveform is 180^0 so it is called "W" PDPWM technique. Seen from Fig. 3.26 [32] it is known that when the modulation waveform intersects the first carrier band, even if the two adjacent intersecting points respectively locate in the carrier waveforms of two different devices, no switching modes conversion occurs at the edge of the two kinds of carrier waveforms, which means no unexpected output levels will emerge when the modulation waveform intersects the second or the third or the fourth carrier band and the two adjacent intersecting points respectively locate in the carrier waveforms of two different devices, switching modes conversions with the same output levels will occur at the edge of the two kinds of carrier waveforms which means unexpected output levels will emerge.

3.6.1   "W" PDPWM AND "M" PDPWM TECHNIQUE

Fig. 3.25 Carrier waveforms and the representative PWM pulse waveforms of the "W" PDPWM technique

In Fig. 3.25 c.f [32], when the modulation waveform intersecting points respectively locate in the carrier waveforms of two different devices, no switching modes conversion occurs at the edge of the two kinds of carrier waveforms, which means no unexpected output level will emerge; when the modulation waveform intersects the first or the second or the third carrier band and the two adjacent intersecting points respectively locate in the carrier waveforms of two different devices, switching modes

conversions with the same output levels will occur at the edge of the two kinds of carrier waveforms, which means unexpected output levels will emerge.

Obviously, if the "M" carriers are applied to the first carrier band and the "W" carriers to the fourth carrier band, the switching modes conversions causing the unexpected output levels can be avoided[4]. On the other hand, in order to avoid the switching modes conversions causing the unexpected output levels for the second and third carrier bands, the carrier cells (triangle waveforms) in opposite phase alternatively are applied to these two carrier bands respectively, as shown in Fig. 3.27 c.f [32], which is called AHPWM (Alternative Hybrid PWM) technique.

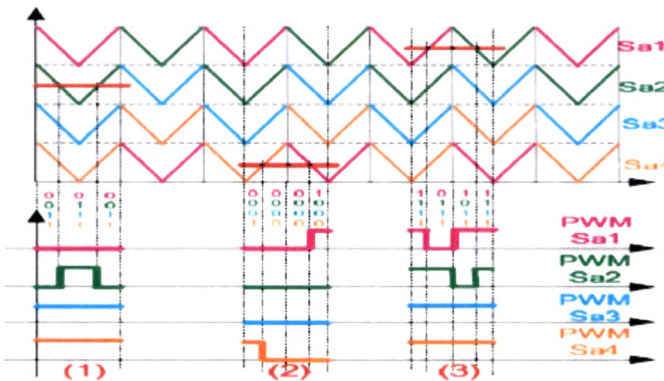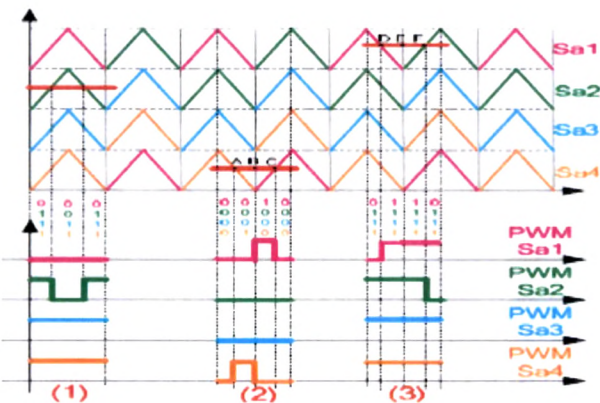**Fig. 3.26 Carrier waveforms and the representative PWM pulse waveforms of the "M" PDPWM technique**
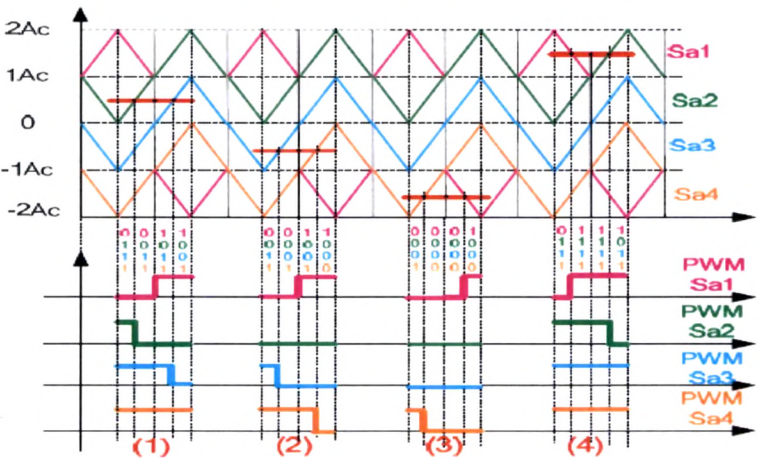

Fig. 3.27 Carrier waveforms and the representative PWM pulse waveforms of AHPWM technique

Fig. 3.27[32] shows four cases of the modulation waveform intersecting four carrier bands respectively. Case "(3)" is similar to the case "(2)" in Fig. 3.25, and case

"(4)" is similar to the case "(3)" in Fig. 3.26 c.f [32], that is to say, no switching modes conversions occur at the edge of two kinds of carrier waveforms with different colors, so no unexpected output levels emerge. In the case of "(1)" and case of "(2)", applying the alternative hybrid carrier cells (triangle waveforms), the switching modes conversions at the edge of two kinds of carrier waveforms with different colors is corresponding to the different output levels respectively, so no unexpected output levels will emerge, which is known from the above analyses [32].

3.7   SPACE VECTOR MODULATION

The space vector modulation technique is based on reconstruction of sampled reference voltage with help of switching space vectors of a voltage source inverter in a sampling period. Each multilevel inverter has several switching states which generate different voltage vectors and can be used to modulate the reference. In SVM, the reference signal is generated from its closest signals. Some vectors have redundant switching states, meaning that they can be generated by more than one switching state this feature is used for balance of capacitor voltages. Multilevel SVM must manage this behavior to optimize the search of the modulating vectors and apply an appropriate switching sequence.

3.7.1 SPACE VECTORS

The space vector modulation (SVM) is also described using symmetrical three-phase systems in the α-ß reference frame. The three-phase reference voltages are represented as a single reference phasor with constant length and angular speed. It substitutes the demanded voltage space vectors by the nearest real voltage space vectors in an appropriate combination in each sampling interval. The basic principles of the SVM is shown in Fig. 3.28 c.f [33] for three level inverter, which involves 27 different inverter switch states (= number of level)^3 [33]. Using a three to two dimensional transformation, the desired output averaged over the switch period and the inverter states are represented as vectors. The visualization and calculation of switching periods is then performed using simple vector math.
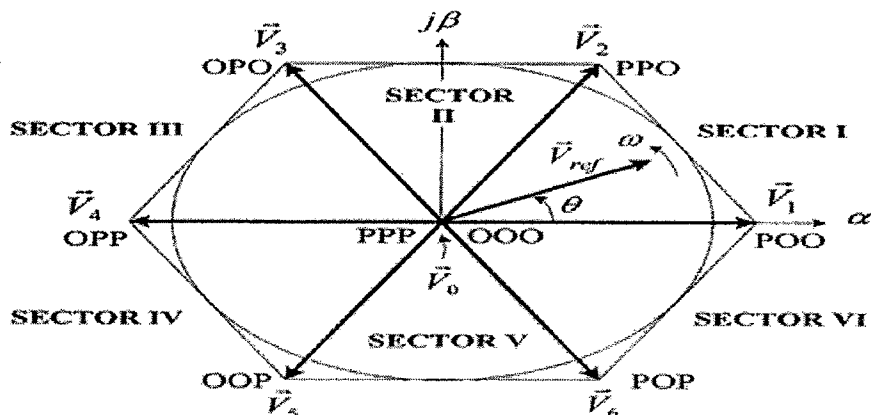
Fig. 3.28 Space vector diagram for the two-level inverter

The voltage common to all three phases can be found at the neutral point of a balanced star connected load. It is known as the zero sequence component. By allowing the neutral point voltage to vary, one phase leg can be held continuously high or low for a 60 degree interval while the other two switch. The correct phase to phase waveforms are still formed. This has two significant advantages.

Firstly, the inverter's full potential modulation depth can be used since the phase to phase voltages are maximized. Secondly, the switching losses are lowered, since the average switching frequency falls to two thirds of its original value. If suitable zero sequence space vectors can be identified for multilevel inverters, the simplicity of multilevel modulator implementations using phase shifted triangular carriers can be retained.

The SVM approach is perhaps the most powerful, because it allows more freedom to control and optimize the switching patterns than any other modulation approach; at the same time, for inverters with higher number of levels it becomes too cumbersome for real-time implementation.

For a given magnitude (length) and position $\overrightarrow{V_{ref}}$ can be synthesized by three nearby stationary vectors, based on which the switching states of the inverter can be selected and gate signals for the active switches can be generated. When $\overrightarrow{V_{ref}}$ passes through sectors one by one, different sets of switches will be turned on or off. As a result, when $\overrightarrow{V_{ref}}$ rotates one revolution in space, the inverter output voltage varies one cycle over time. The inverter output frequency corresponds to the rotating speed of $\overrightarrow{V_{ref}}$ while its output voltage can be adjusted by the magnitude of $\overrightarrow{V_{ref}}$.

The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period Ts of the modulation scheme. The dwell time calculation is based on 'volt-second balancing' principle, that is, the product of the reference voltage $\overrightarrow{V_{ref}}$ and sampling period Ts equals the sum of the voltage multiplied by the time interval of chosen space vectors. When $\overrightarrow{V_{ref}}$ falls into sector I as shown in Fig. 3.29 c.f [33] it can be synthesized by $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_0}$.

Table 3.1 Space Vectors, Switching States, and On-State Switches

Space Vector	Switching State (Three Phases)	On-State Switch	Vector Definition
$\overrightarrow{V_0}$	[PPP] [OOO]	S1, S3, S5 S4, S6, S2	$\overrightarrow{V_0} = 0$
$\overrightarrow{V_1}$	[POO]	S1, S6, S2	$\overrightarrow{V_1} = \dfrac{2}{3} V_d\, e^{j0}$
$\overrightarrow{V_2}$	[PPO]	S1, S3, S2	$\overrightarrow{V_2} = \dfrac{2}{3} V_d\, e^{j\frac{\pi}{3}}$
$\overrightarrow{V_3}$	[OPO]	S4, S3, S2	$\overrightarrow{V_3} = \dfrac{2}{3} V_d\, e^{j\frac{2\pi}{3}}$
$\overrightarrow{V_4}$	[OPP]	S4, S3, S5	$\overrightarrow{V_4} = \dfrac{2}{3} V_d\, e^{j\frac{3\pi}{3}}$
$\overrightarrow{V_5}$	[OOP]	S4, S6, S5	$\overrightarrow{V_5} = \dfrac{2}{3} V_d\, e^{j\frac{4\pi}{3}}$
$\overrightarrow{V_6}$	[POP]	S1, S6, S5	$\overrightarrow{V_6} = \dfrac{2}{3} V_d\, e^{j0\frac{5\pi}{3}}$

The coefficient 2/3 is somewhat arbitrarily chosen. The commonly used value is 2/3 or √2/3. The main advantage of using 2/3 is that the magnitude of the two-phase voltages will be equal to that of the three-phase voltages after the transformation. A space vector can be generally expressed in terms of the two-phase voltages in the α-ß plane. The zero vector $\overrightarrow{V_0}$ has two switching states [PPP] and [OOO], one of which seems redundant. The redundant switching state can be utilized to minimize the switching frequency of the inverter or perform other useful functions. Note that the zero and active vectors do not move in space, and thus they are referred to as stationary vectors. On the contrary, the reference vector $\overrightarrow{V_{ref}}$ in Fig. 3.29 rotates in space at an angular velocity $\omega = 2\pi f_1$

where $f1$ is the fundamental frequency of the inverter output voltage.

The angular displacement between $\overrightarrow{V_{ref}}$ and the α axis of the α-ß plane can be obtained by $\theta(t) = \int_0^t \omega(t)dt + \theta(0)$

With the space vectors selected and their dwell times calculated, the next step is to arrange switching sequence. In general, the switching sequence design for a given $\overrightarrow{V_{ref}}$ is not unique, but it should satisfy the following two requirements for the minimization of the device switching frequency: (a) The transition from one switching state to the next involves only two switches in the same inverter leg, one being switched on and the other switched off. (b) The transition for $\overrightarrow{V_{ref}}$ moving from one sector in the space vector diagram to the next requires no or minimum number of switchings.
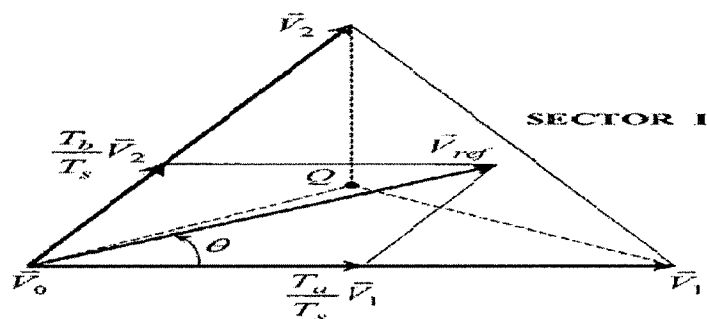

Fig. 3.29 $\overrightarrow{V_{ref}}$ synthesized by $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_0}$

3.7.2 SWITCHING SEQUENCE

Fig. 3.30 c.f [33] shows a typical seven-segment switching sequence and inverter output voltage waveforms for $\overrightarrow{V_{ref}}$ in sector I, where $\overrightarrow{V_{ref}}$ is synthesized by $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_0}$. The sampling period Ts is divided into seven segments for the selected vectors.
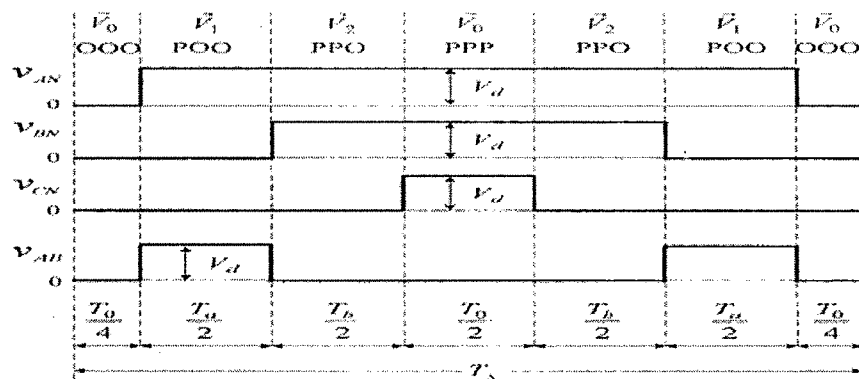

Fig.3.30 Seven-segment switching sequence for $\overrightarrow{V_{ref}}$ in sector I
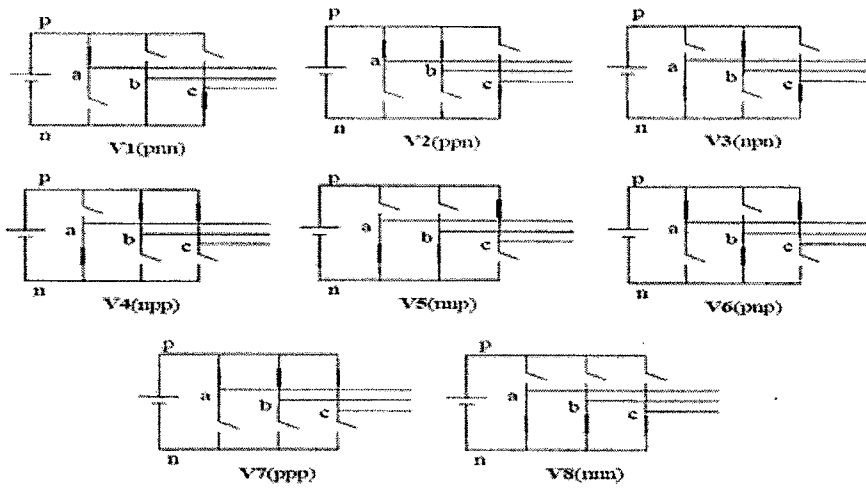
Fig. 3.31 Eight switching state topologies of a voltage source inverter

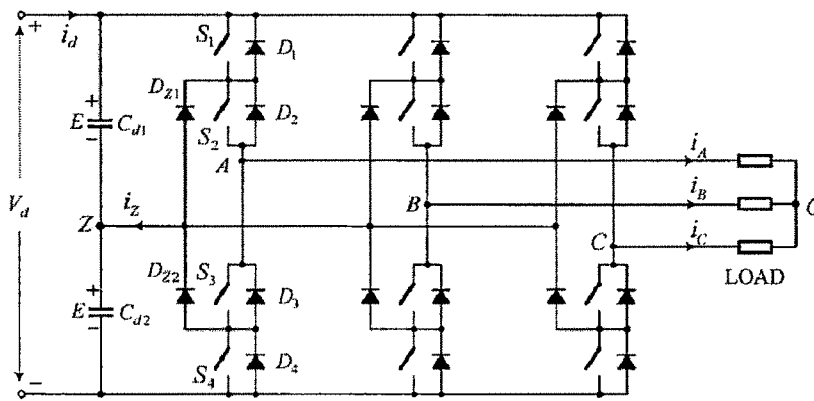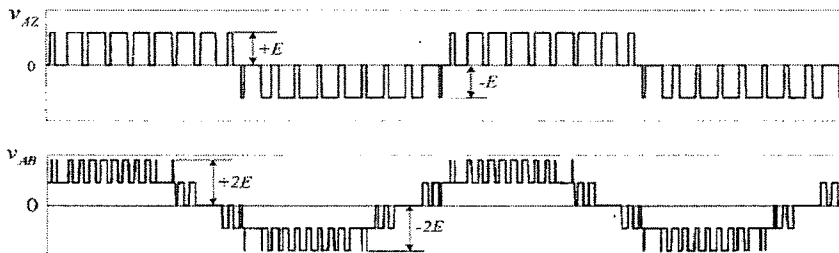Fig. 3.32 Three-level NPC inverter

Fig. 3.33 Output voltage waveforms of the NPC inverter

The line-to-line voltage waveform produced by the SVM inverter contains even-order harmonics which can be eliminated by modified SVM scheme. As the switching sequence design is not unique for a given set of stationary vectors and dwell times, switching discontinuity can give discontinuous space vector modulation.

3.8   COMPARISON OF MODULATION TECHNIQUES ON BASIS OF MODULATION INDEX

It is observed that THD varies with type of inverter topology, output level and modulation index. Generally variability in THD is about 10% for different modulation techniques [1-34].

Table 3.2 Modulation techniques summarized

Sr. No	Modulation Technique	Output Voltage level	Topology(Diode Clamped, Flying Capacitor, Cascaded MLI or Hybrid MLI)	THD (Approx) %
1	Phase Disposition (PD) Technique	5 9 7 5	NPC Asymmetrical MLI Hybrid cascaded MLI Cascaded MLI	13 15.7 6.5/5.23 5.2
2	Phase Opposition Disposition (POD) Technique	5	Cascaded MLI	6.56 6.8
3	Alternative Phase Opposition Disposition (APOD)	5	Cascaded MLI	5.68 12.9
4	Phase Shifted (PS) Technique	5	Cascaded MLI	9.72
5	Hybrid modulation techniques	9	Hybrid MLI	13.96
6	Optimized Hybrid PDPWM	7 9 11	Cascaded MLI	17.19 12.87 9.95
7	ISPWM	7	Asymmetric Cascaded Multilevel Inverter	7.98
8	VFISPWM	7	Hybrid MLI	5.92
9	Multi carrier switching frequency optimal PWM (MC-SFO PWM)	5	Cascaded	21.5
10	Phase Shifted Carrier Switching Frequency Optimal Pulse Width Modulation (PSC-SFO PWM)	5	Cascaded	20.5
11	Phase-Shifted Suboptimal Carrier PWM (PS-SUB-PWM)	5	Cascaded	.22
12	Higher and Lower Carrier Cells and Alternative Phase Opposition PWM (HLCCAPOPWM)	5	Hybrid MLI	38.6
13	Alternative hybrid PWM (AHPWM)	5	Hybrid MLI	35.95
14	SPACE VECTOR MODULATION PD POD APOD	5	Cascaded	4.45 5.23 10.38

Some modulation techniques are easy to implement but as in hybrid modulation technique if it is implemented directly i.e. by using low frequency and high frequency

modulation with constant carrier frequency then THD is higher as compared with ISPWM, VFISPWM or optimized hybrid PWM. Similarly as the complication of generating and implementing of modulation techniques is increased THD decreases. Also some modulation techniques can be directly applied to multilevel inverters like NPC but modifications are required for implementing same technique to hybrid multilevel inverter. Comparison is briefly summarized in Table 3.2.

Space vector modulation technique has more degree of freedom in control and optimization of switching pattern as compared to other techniques. But at the same time its real time implementation is difficult for multilevel inverters with higher number of levels. HLCCAPOPWM and alternative hybrid modulation techniques are related with PDPWM and THD obtained is not much low but it can be further improved by taking appropriate modulation index. Thus various modulation techniques can be used directly or hybrid technique can be applied for hybrid multilevel inverter.

3.9   SUMMARY

The different modulation techniques are discussed in this chapter. It is observed that total harmonic distortion changes with inverter topology, output levels of multilevel inverter and modulation index. Some modulation techniques are easy to implement but as in hybrid modulation technique if it is implemented directly i.e by using low frequency and high frequency modulation with constant carrier frequency then THD is higher as compared to ISPWM, VFISPWM or optimized hybrid PWM. Similarly as the complexity of generation and implementation of modulation techniques is increased THD is likely to be decreases. Also some modulation techniques can be directly applied to multilevel inverters like NPC but modifications are required for implementing same technique to hybrid multilevel inverter.

The optimization in modulating signal as discussed in SFO-PWM only has the value to increase the available linear modulation region. While in PSC SFO PWM the zero sequence modification technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs. Also the PSSUB- PWM is suitable for three-phase systems, as harmonics added are triplens and in three phase system triplens are missing. HLCCAPOPWM and alternative hybrid modulation techniques are related with PDPWM and THD obtained is not much low but it can be further improved by taking appropriate modulation index.