CHAPTER 4

SIMULATIONS RESULTS for MULTILEVEL INVERTER and HYBIRD MULTILEVEL INVERTER

In this chapter MATLAB simulations done for different cascaded multilevel inverters (CMLI) and hybrid multilevel inverters (HMLI) are described and analyzed. Simulations are carried out for 5 level, 7 level and 9 level output with respect to cascaded multilevel inverter. Different modulation techniques implemented are PD, POD, APOD and hybrid modulation technique. Modulation index is taken either 0.9 or 1 specified with respective output figures while frequency modulation index is 21. For better visualization figures are resolved, but simulations and THD measurement are done as per the values specified. Further sections describe MATLAB simulations for different MLI and HMLI.

4.1 SIMULATIONS FOR CASCADED MULTILEVEL INVERTER

As per the theory discussed in chapter 2 and chapter 3 simulations are carried out for different cascaded multilevel inverter and FFT analysis is done in MATLAB/SIMULINK to obtain THD.

4.1.1 FIVE LEVEL CASCADED MULTILEVEL INVERTER

As shown in Fig. 4.1 if two H bridges are cascaded then 5 level output is obtained. Though practically type of switches used do make difference in output but in simulations no major difference is observed.

4.1.1.1 Five Level Cascaded Multilevel Inverter with Staircase Technique

Fig. 4.1 shows block diagram structure in MATLAB/SIMULINK for 5 level cascaded MLI.

For all simulation results on Y-axis voltage in volts is taken and on X-axis time is taken in seconds.

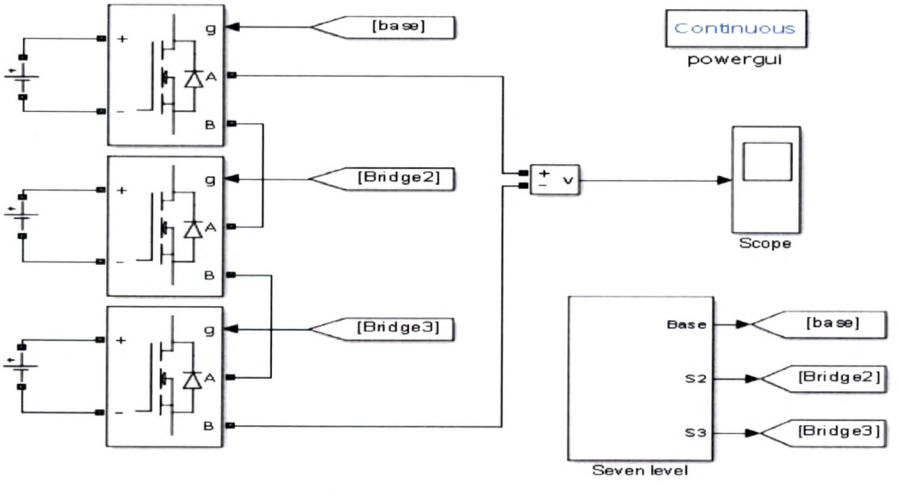

Fig. 4.1 Simulink block for cascaded multilevel inverter

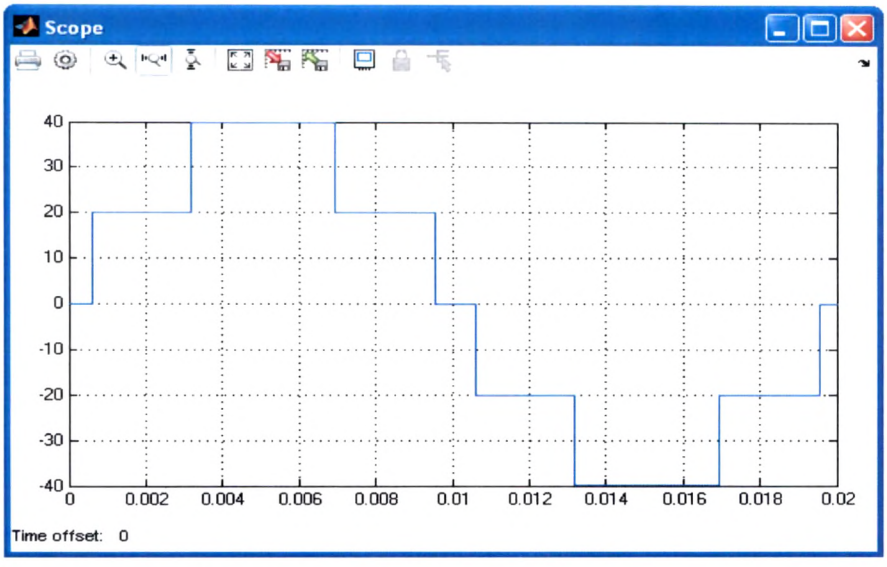

Fig. 4.2 Simulink output for five level cascaded multilevel inverter

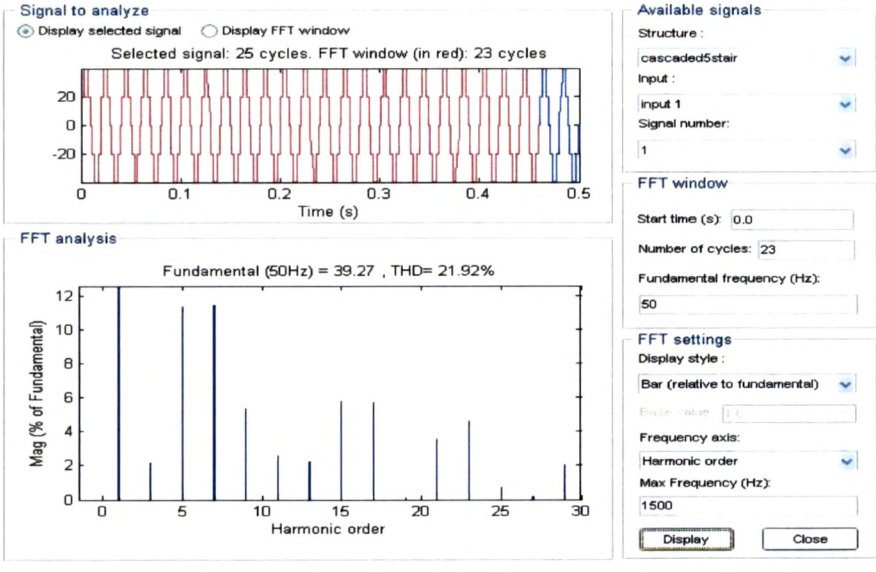

Fig. 4.3 FFT analysis and THD for five level cascaded multilevel inverter

In this simulation universal bridge simulink block is used in which MOSFET switch is chosen. Fig. 4.2 shows 5 level output voltage where V_{dc} is 20V for each bridge thus DC voltage is equal for both bridges. MOSFETs are switched at approximately 10^0 and 56^0 to obtain V_{dc} and $2V_{dc}$ as the output, accordingly rest of switching takes place. Switching angles can be obtained using different techniques such as selective harmonic elimination (SHE).

Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.3 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

4.1.1.2 Five Level Cascaded Multilevel Inverter with Phase Disposition Modulation Technique

Block diagram structure for 5 level cascaded MLI with PD modulation technique remains same as Fig. 4.1. Control block is changed as shown in Fig. 4.4 where 'g1'-'g2' combine to give 'A' and 'g5'-'g6' combine to give 'A1' in Fig. 4.1. Fig. 4.5 shows carrier and modulating signal for PD modulation technique for five level cascaded MLI. Modulation index is specified earlier. Fig. 4.6 shows 5 level output voltage where V_{dc} is 20V for each bridge. Thus DC voltage is equal for both bridges. Thus output can be changed with different modulation index for amplitude and frequency hence THD will change accordingly. Fig. 4.7 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

Similar outputs can be obtained for POD and APOD modulation technique.

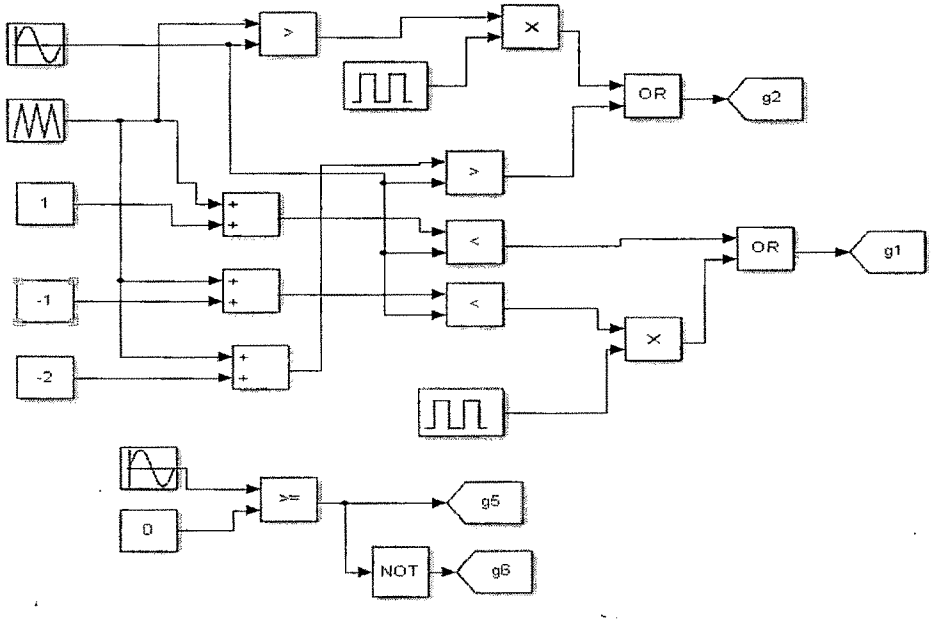

Fig. 4.4 Control block for five level cascaded MLI with PD technique

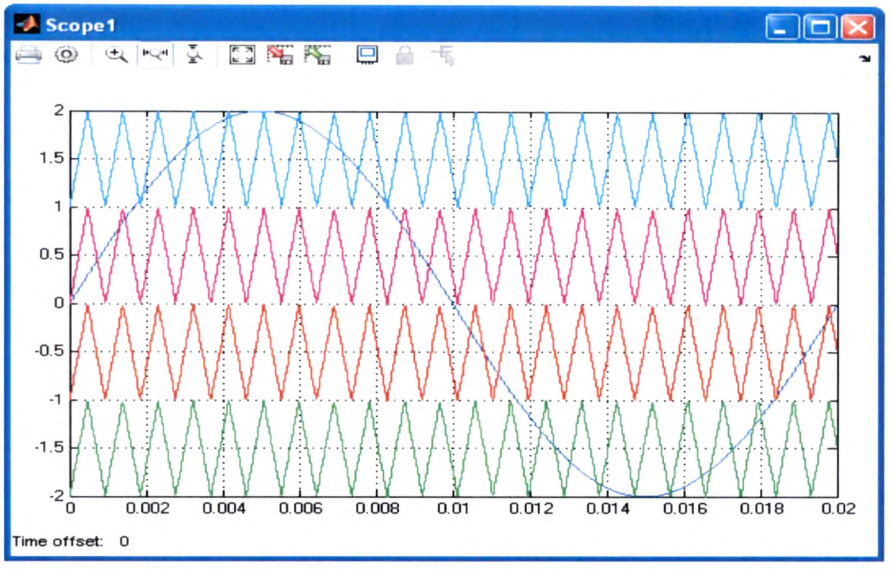

Fig. 4.5 Carrier and modulating signal for five level cascaded MLI with PD technique

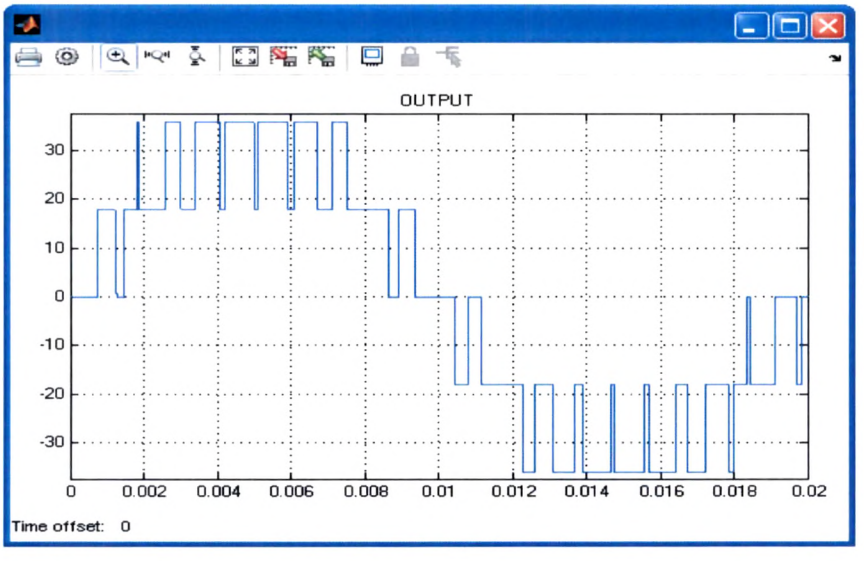

Fig. 4.6 Simulink output for five level cascaded multilevel inverter with PD technique

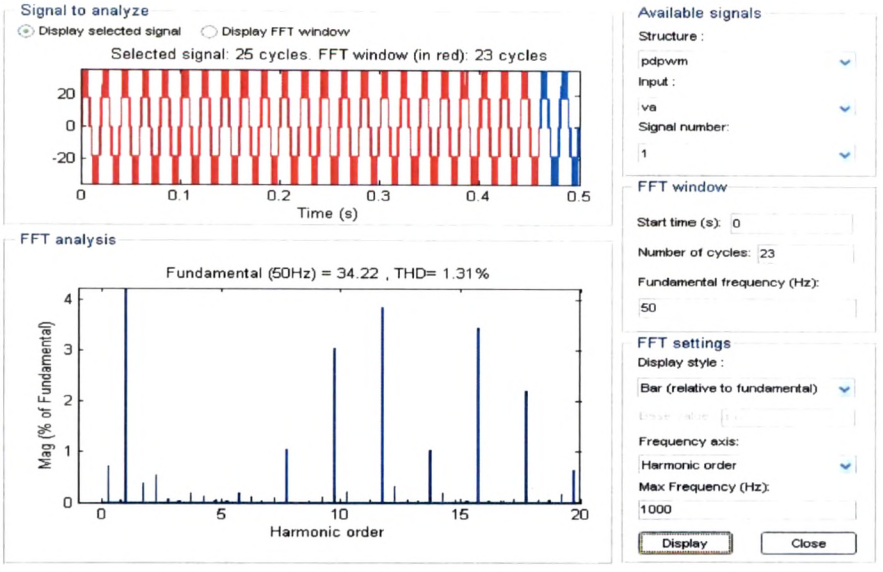

Fig. 4.7 FFT analysis and THD for five level cascaded multilevel inverter with PD technique

4.1.2 SEVEN LEVEL CASCADED MULTILEVEL INVERTER

Seven level output can be obtained using two or three H bridges by varying V_{dc} as per requirement.

4.1.2.1 Seven Level Cascaded Multilevel Inverter with Staircase Technique Using Three H Bridges

A) Using three bridges

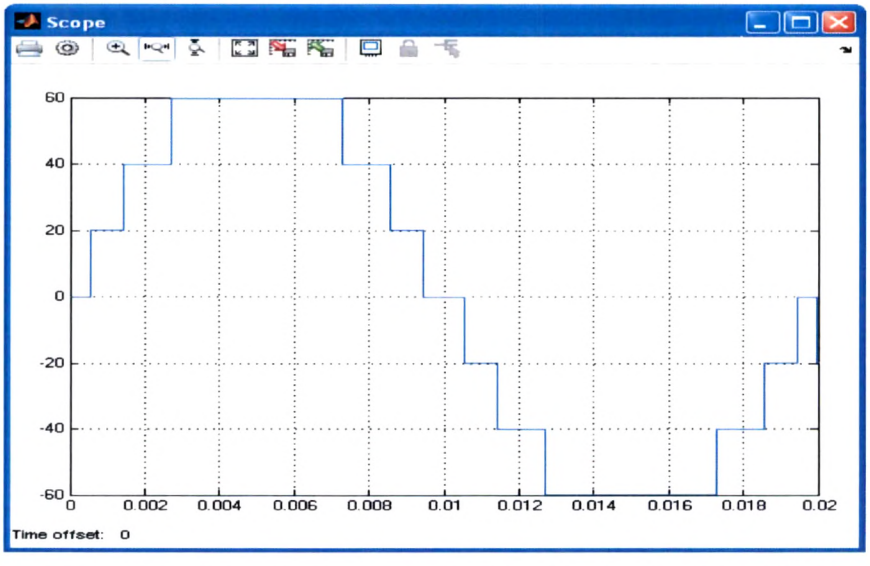

Fig. 4.8 Simulink output for seven level CMLI using three H bridges

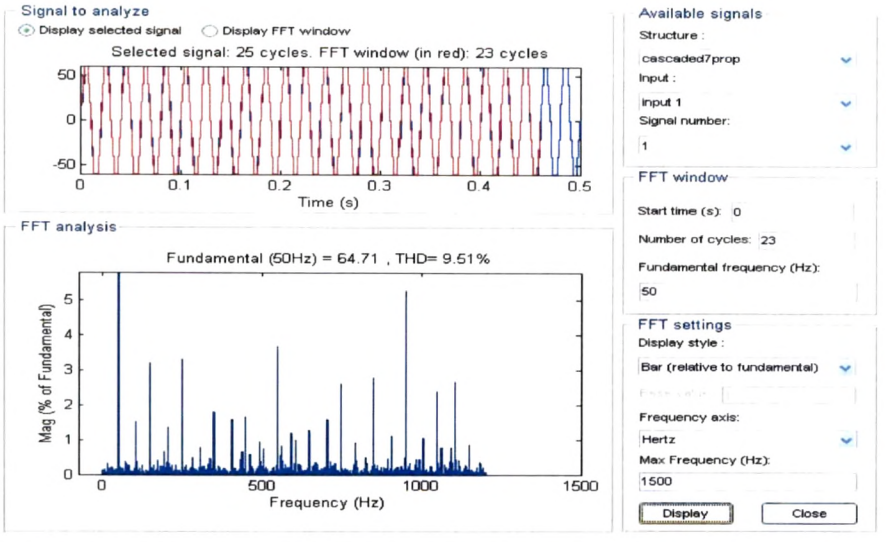

Fig. 4.9 FFT analysis and THD for seven level CMLI for specified angles

Block diagram structure for 7 level cascaded MLI with three H bridges is shown in Fig. 4.1. Switches are switched at approximately 10^0, 26^0 and 49^0 to obtain V_{dc}, $2V_{dc}$ and $3V_{dc}$ and accordingly rest of switching takes place. Fig. 4.8 shows 7 level output voltage where V_{dc} is 20V for each bridge thus DC voltage is equal for all bridges. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.9 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency.

B) Using two bridges

Fig. 4.10 Simulink output for 7 level CMLI using 2 H bridges

Seven level cascaded MLI with two H bridges can be obtained by removing one H bridge from Fig. 4.1 and changing DC voltages to V_{dc} and $2V_{dc}$. Switches are switched at approximately 10^0, 26^0 and 49^0 to obtain V_{dc}, $2V_{dc}$ and 3 V_{dc} and accordingly rest of switching takes place. Fig. 4.10 shows 7 level output voltage where V_{dc} is unequal for H bridges. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.11 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

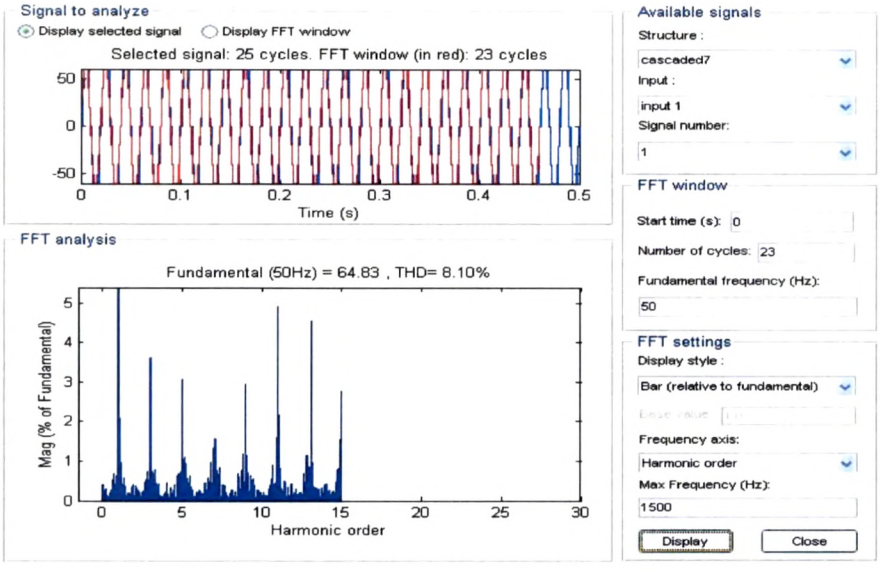

Fig. 4.11 FFT analysis and THD for 7 level CMLI for specified angles

4.1.2.2 Seven Level Cascaded Multilevel Inverter with Phase Disposition Modulation Technique

A) Using three bridges

Block diagram structure for 7 level cascaded MLI with PD modulation technique remains same as Fig. 4.1. Control block will consist of carrier and modulating signal for PD technique with number of carriers increased to six as output is having seven levels As shown in Fig. 4.5 number of carriers is increased while modulating signal is same. Modulation index is specified earlier. Fig. 4.12 shows 7 level output voltage where V_{dc} is 20V for each bridge, the DC voltage is equal for all bridges. Thus output can be changed with different modulation index for amplitude and frequency hence THD will change accordingly. Fig. 4.13 corresponds to FFT analysis giving THD at 23rd cycle with 1000 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

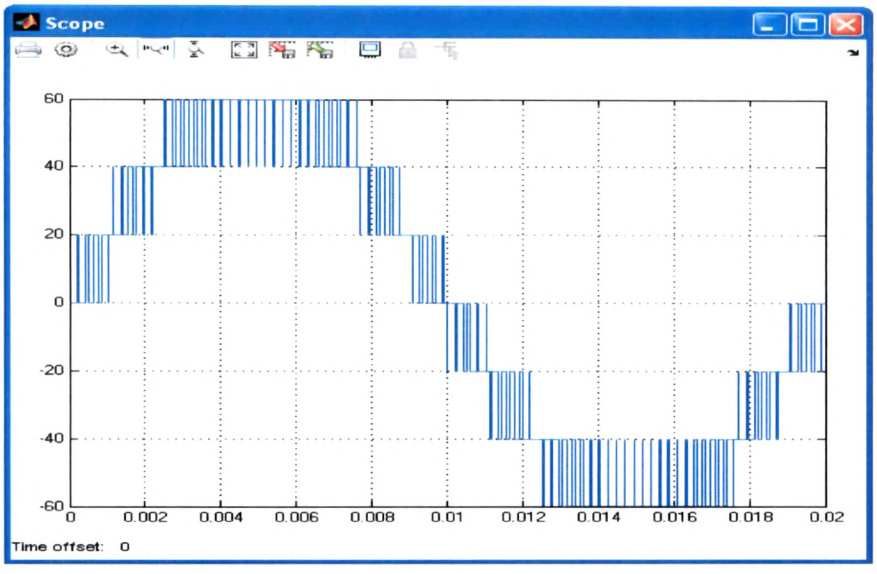

Fig. 4.12 Simulink output for 7 level CMLI with PD technique

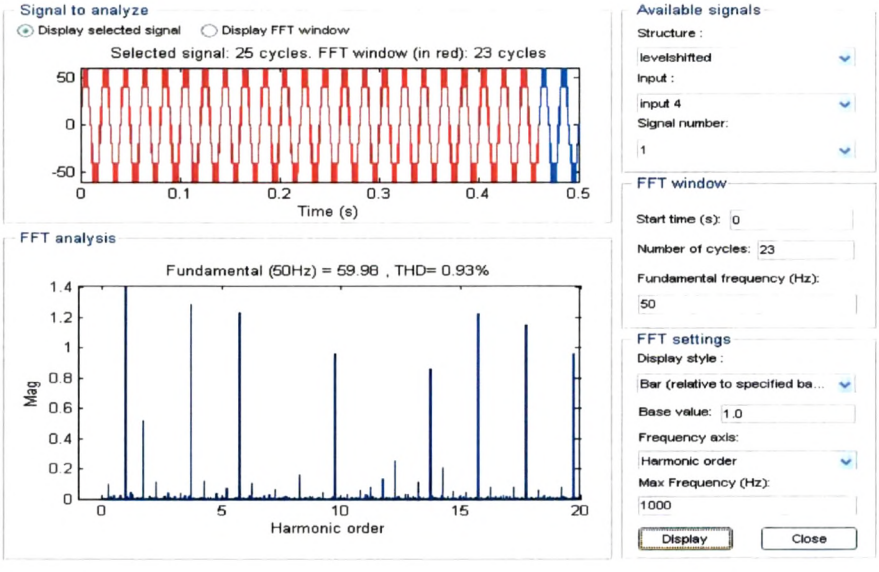

Fig. 4.13 FFT analysis and THD for seven level cascaded multilevel inverter with PD technique

Similar outputs can be obtained for POD and APOD modulation technique as shown in Fig. 4.14 and Fig. 4.15 respectively.

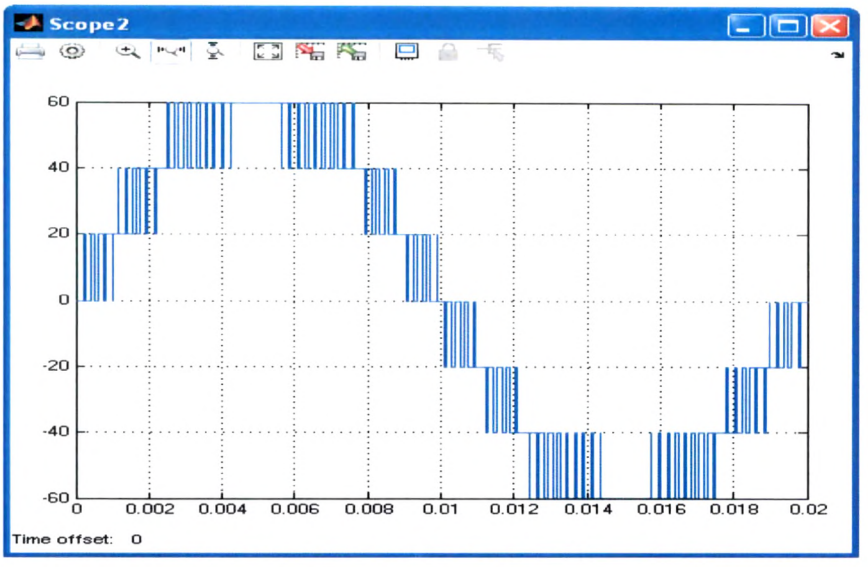

Fig. 4.14 Simulink output for 7 level CMLI with POD technique

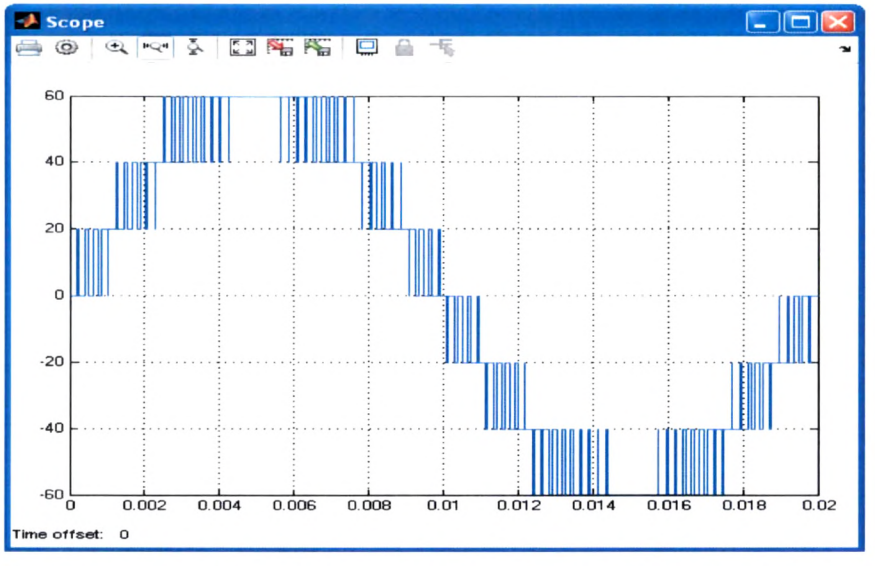

Fig. 4.15 Simulink output for 7 level CMLI with APOD technique

4.1.3 NINE LEVEL CASCADED MULTILEVEL INVERTER

Nine level output can be obtained by using two or four H bridges by varying V_{dc} as per requirement.

4.1.3.1 Nine Level Cascaded Multilevel Inverter with Staircase Technique Using Three H Bridges

A) Using four bridges

Switches are switched at approximately 7.5^0, 19.1^0, 33.5^0 and 51.6^0 to obtain V_{dc}, $2V_{dc}$, $3V_{dc}$ and $4V_{dc}$ and accordingly rest of switching takes place. Fig. 4.16 shows 9

level output voltage where V_{dc} is 20V for each bridge thus DC voltage is equal for all bridges. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.17 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

Block diagram structure for 9 level CMLI with four H bridges can be obtained by adding one H bridge Fig. 4.1.

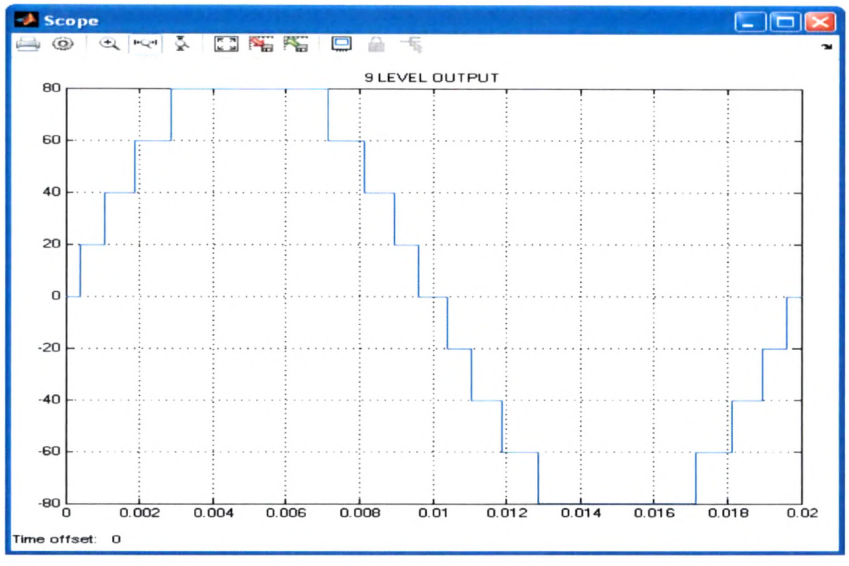

Fig. 4.16 Simulink output for 9 level CMLI for 4 H bridges

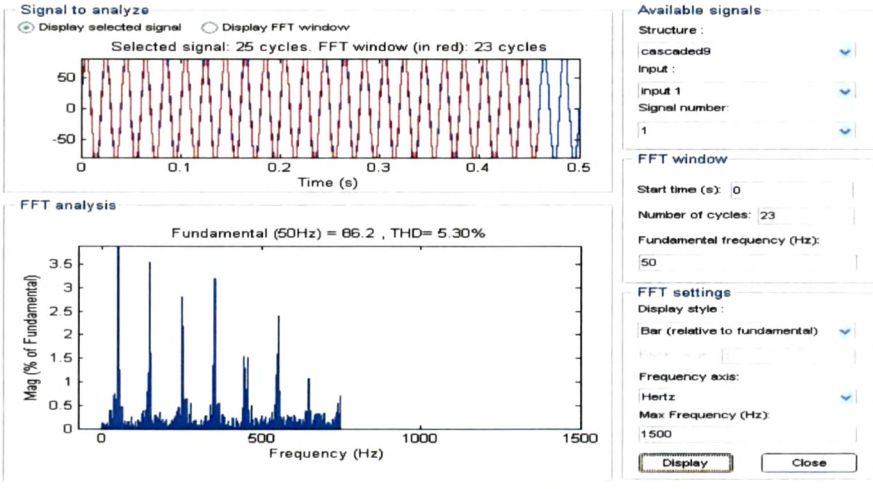

Fig. 4.17 FFT analysis and THD for 9 level CMLI for specified angles

B) Using two bridges

Nine level cascaded MLI with two H bridges can be obtained by removing one

H bridge from Fig. 4.1 and changing DC voltages to V_{dc} and $3V_{dc}$.

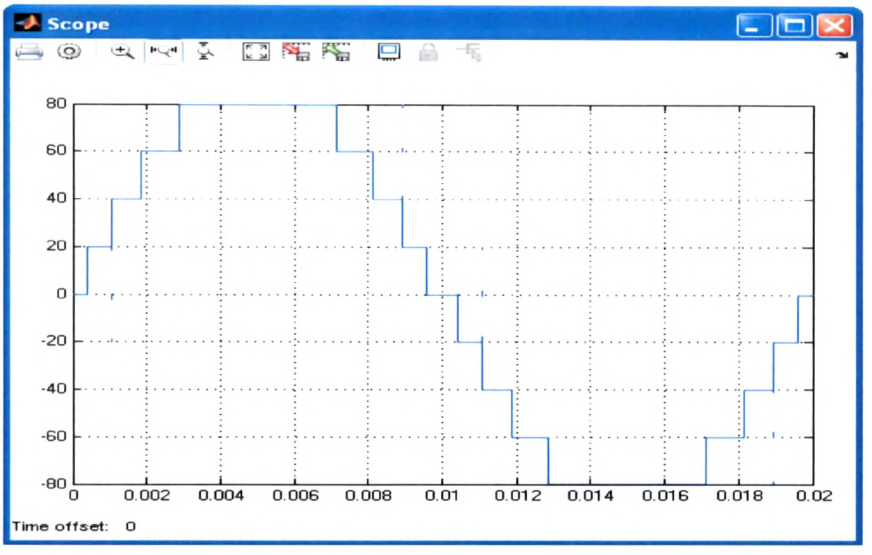

Fig. 4.18 Simulink output for nine level cascaded multilevel inverter for 2 H bridges

Switches are switched at approximately 7.5^0, 19.1^0, 33.5^0 and 51.6^0 to obtain 0, V_{dc}, $2V_{dc}$ and $3V_{dc}$ and accordingly rest of switching takes place. Fig. 4.18 shows 9 level output voltage where output levels are obtained by addition or subtraction of applied DC voltage i.e. 10V and 30V. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.19 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency.

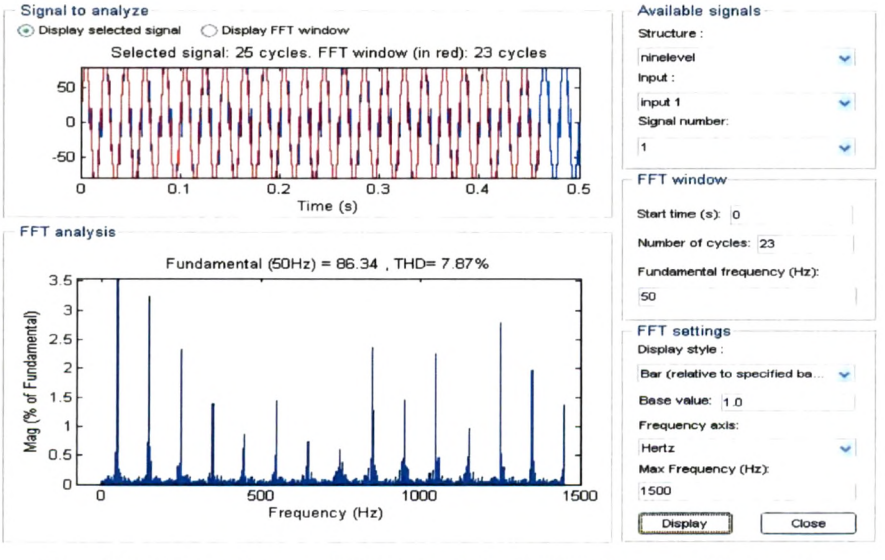

Fig. 4.19 FFT analysis and THD for 9 level CMLI for specified angles

4.2 SIMULATIONS FOR HYBRID MULTILEVEL INVERTER

As per the theory discussed in chapter 2 and chapter 3 simulations are carried out for different hybrid multilevel inverters and FFT analysis is done in MATLAB/SIMULINK to obtain THD.

4.2.1 ASYMMETRIC HYBRID MULTILEVEL INVERTER

As shown in Fig. 4.24 IGBT H bridge is cascaded with GTO H bridge thus giving asymmetric topology with respect to power devices, but in simulations no major difference is observed as compared to cascaded multilevel inverter with same type of power devices.

4.2.1.1 Single Phase Asymmetric Hybrid Multilevel Inverter with Hybrid Modulation Technique

A) Equal DC sources

Fig. 4.20 shows block diagram structure in MATLAB/SIMULINK for asymmetric hybrid multilevel inverter with equal DC sources. Fig. 4.21 is control block and Fig. 4.22 control signals for IGBT and GTO bridge. As per Fig. 4.22 it is observed that GTO H-bridge is switched at low frequency while IGBT bridge is switched at high frequency.

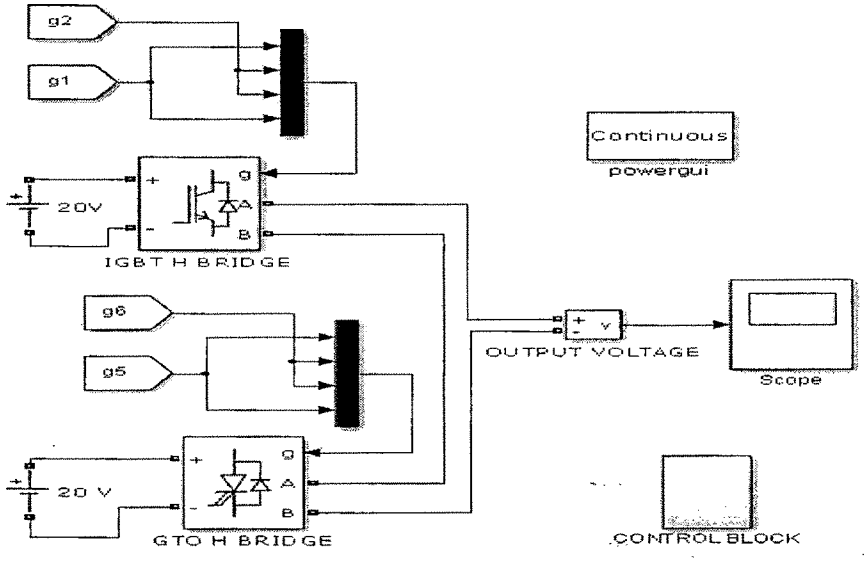

Fig. 4.20 Simulink block for single phase asymmetric hybrid multilevel inverter

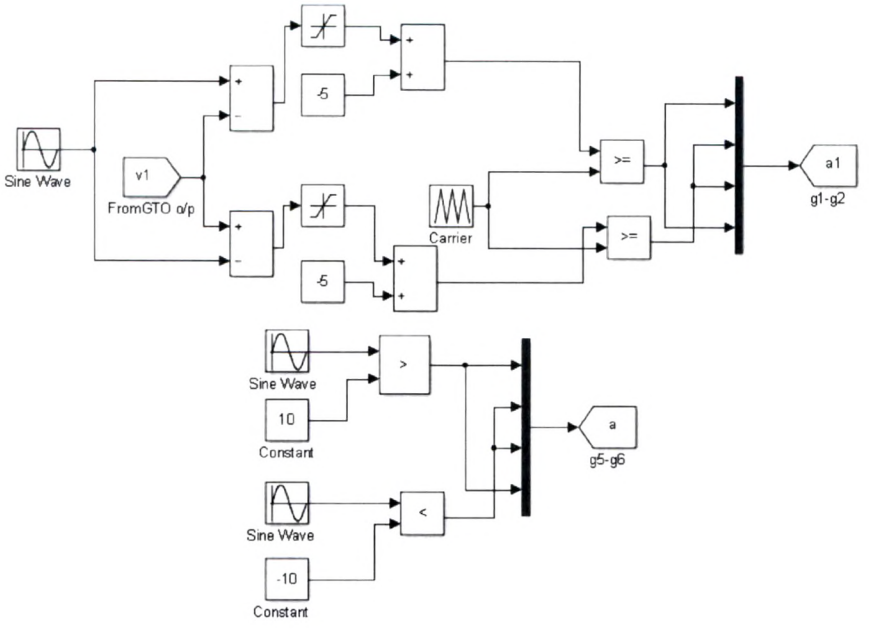

Fig. 4.21 Control block for single phase asymmetric hybrid multilevel inverter with hybrid modulation technique

As DC voltages sources are equal output is five level output as shown in Fig. 4.23. Fig. 4.24 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

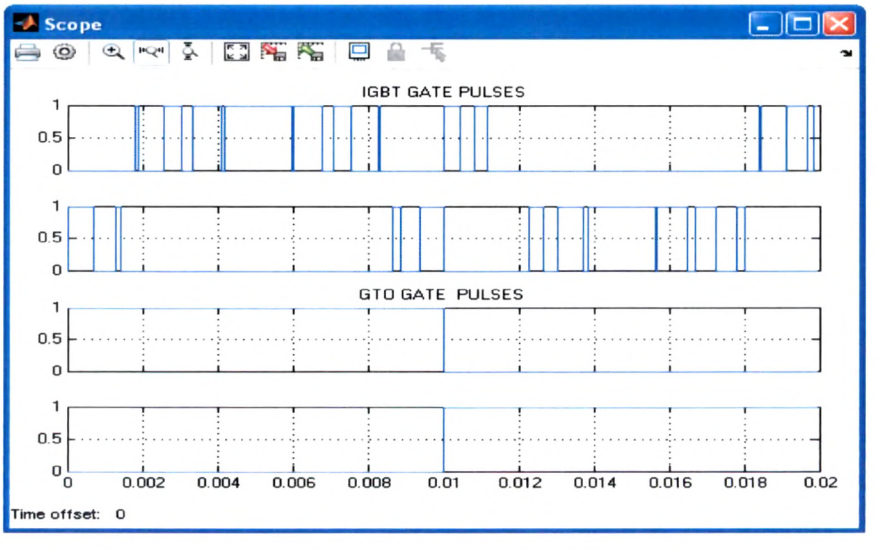

Fig. 4.22 Control signals for asymmetric hybrid multilevel inverter

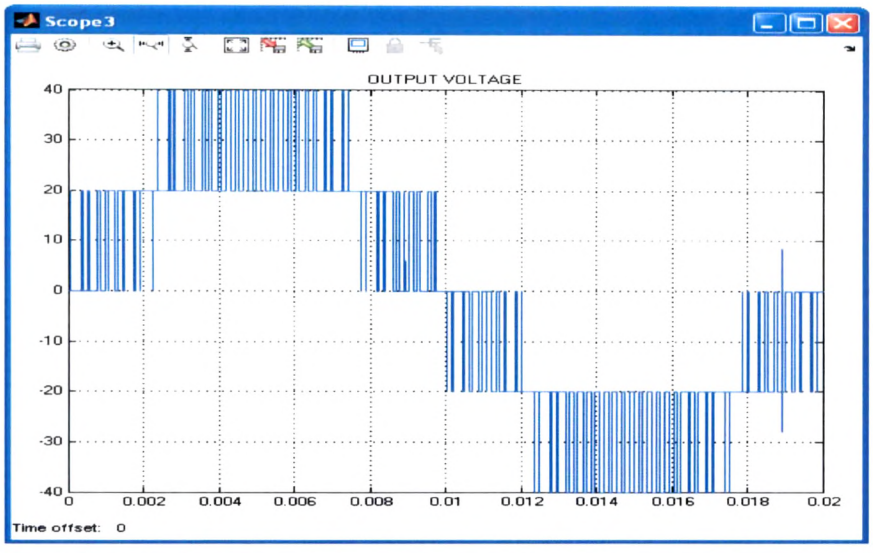

Fig. 4.23 Simulink output for single phase asymmetric multilevel inverter with hybrid modulation technique for equal DC sources

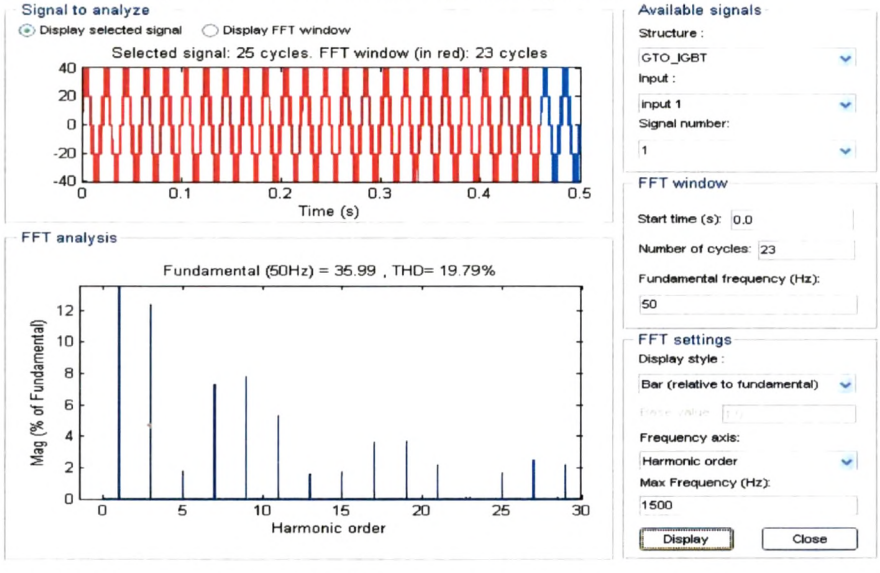

Fig. 4.24 FFT analysis and THD for asymmetric hybrid multilevel inverter with hybrid modulation technique for equal DC sources

B) Unequal DC sources

Asymmetric hybrid multilevel inverter with unequal DC sources is obtained by changing DC sources in Fig. 4.21 as 10V for IGBT H bridge and 20V for GTO H bridge. Control signals are same as shown in Fig. 4.22. As DC voltages sources are unequal output is seven level output as shown in Fig. 4.25. Fig. 4.26 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same

for all analysis unless and until specified. It is observed that if DC voltage value is increased like 100V or more THD remains unchanged in simulation

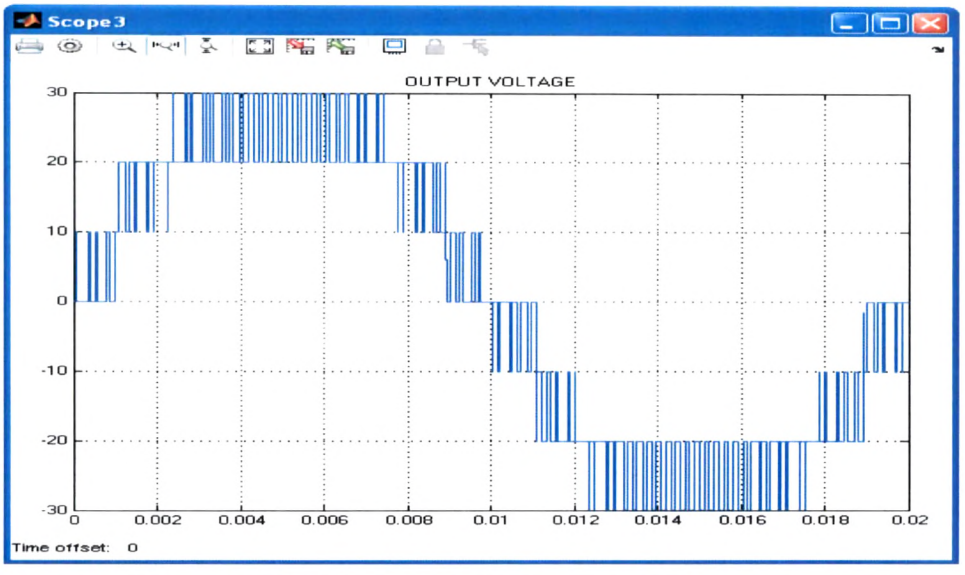

Fig. 4.25 Simulink output for single phase asymmetric multilevel inverter with hybrid modulation technique for unequal DC sources.

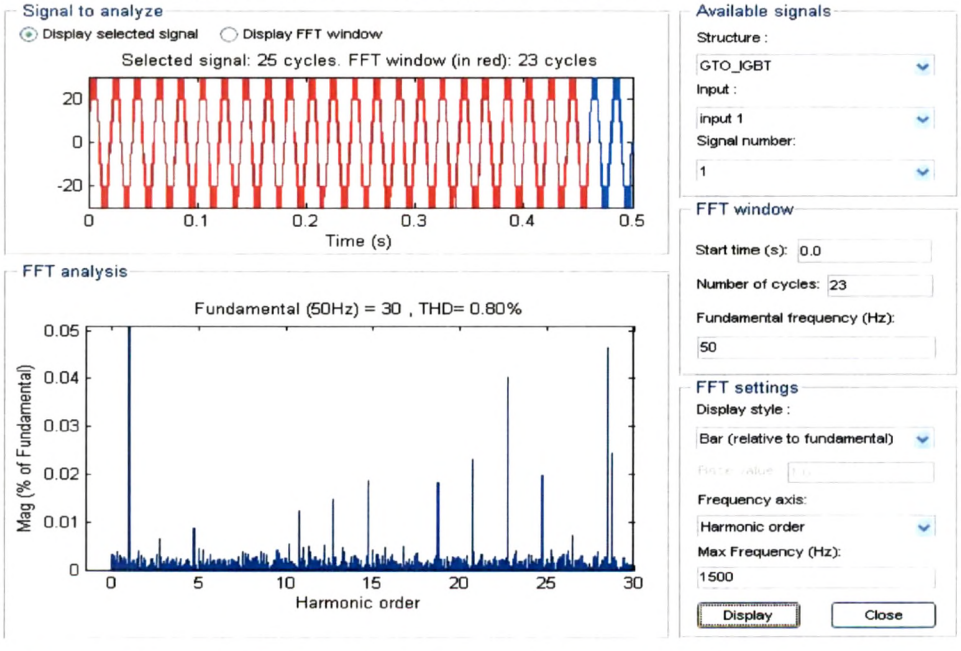

Fig. 4.26 FFT analysis and THD for asymmetric hybrid multilevel inverter with hybrid modulation technique for unequal DC sources

4.2.1.2 Single Phase Asymmetric Hybrid Multilevel Inverter with Phase Disposition Modulation Technique

A) Equal DC sources

Fig. 4.27 shows the output for single phase asymmetric hybrid multilevel inverter with phase disposition modulation technique and equal DC sources which is equal to 20V. Thus five level output is obtained. While Fig. 4.28 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

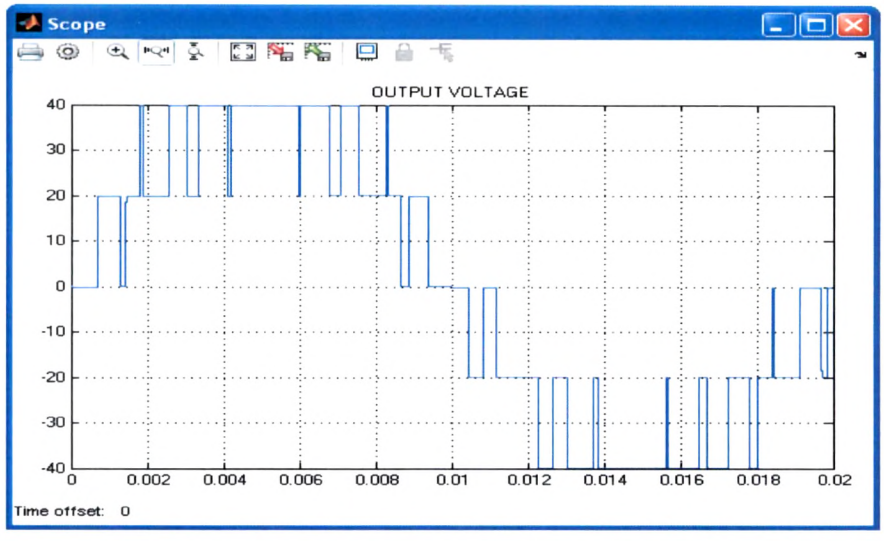

Fig. 4.27 Simulink output for single phase asymmetric multilevel inverter with PD technique for equal voltages

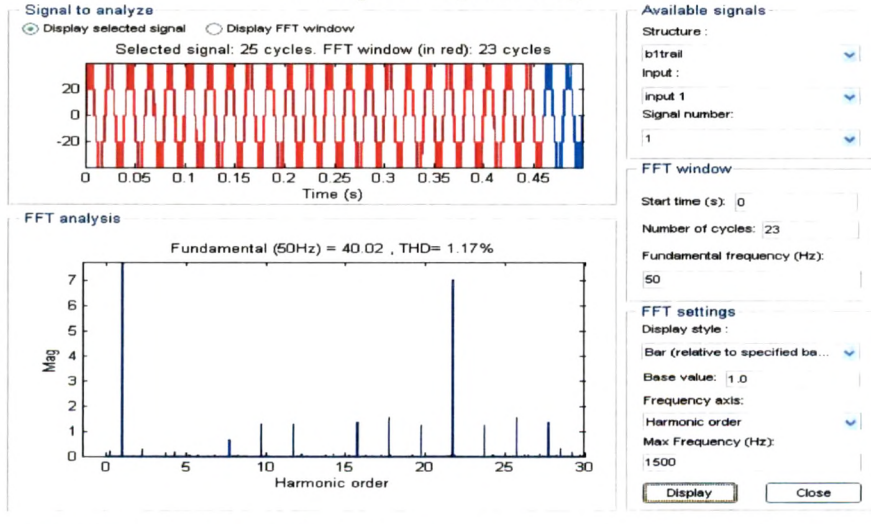

Fig. 4.28 FFT analysis and THD for asymmetric hybrid multilevel inverter with PD modulation technique for equal DC sources

4.2.1.3 Three Phase Asymmetric Hybrid Multilevel Inverter with Hybrid Modulation Technique

A) Equal DC sources

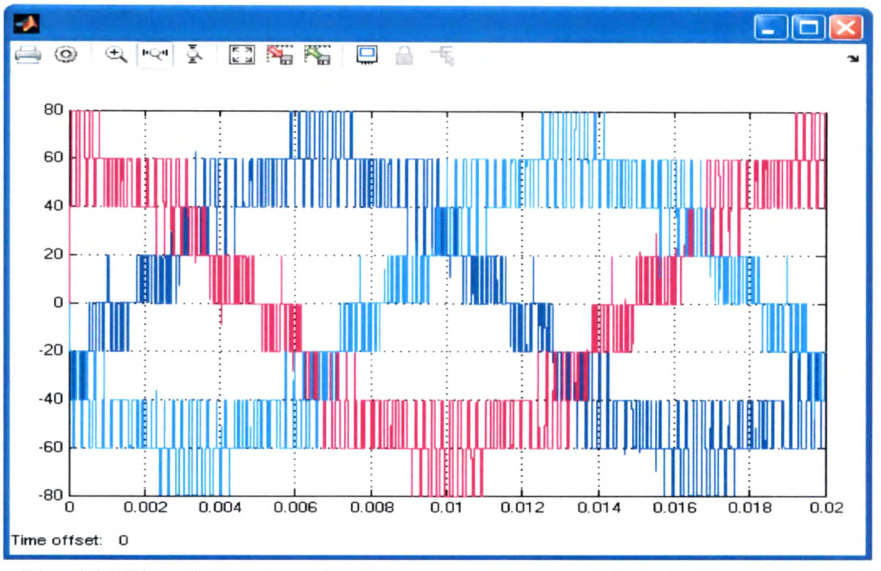

Fig. 4.29 Simulink output for three phase asymmetric hybrid multilevel inverter hybrid modulation technique with equal voltages

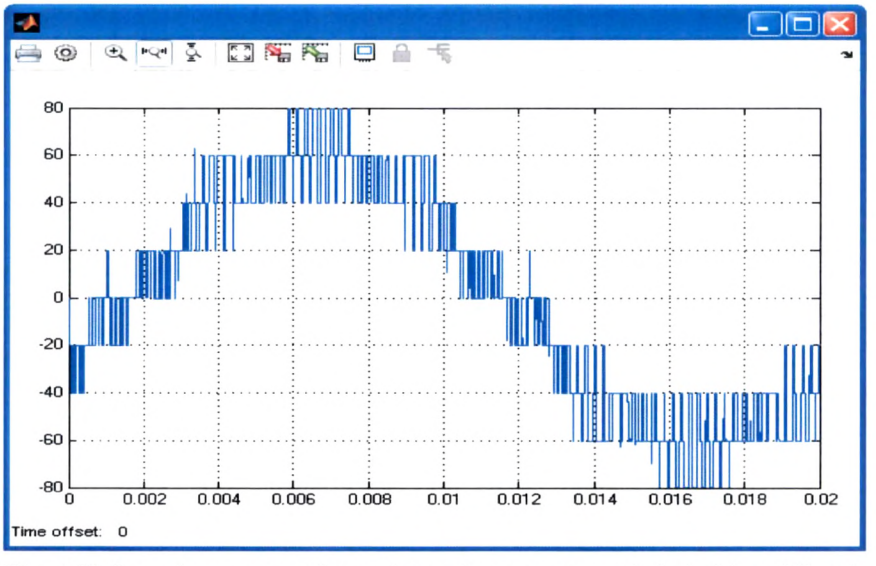

Fig. 4.30 One phase output from three phase asymmetric hybrid multilevel inverter hybrid modulation technique with equal voltages

Fig. 4.29 shows the output for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique and equal DC sources where voltage is 20V. In three phase control signals are phase shifted by 120^0. Fig. 4.30 shows nine level output for single leg of three phase asymmetric hybrid multilevel inverter. While Fig.4.31

corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

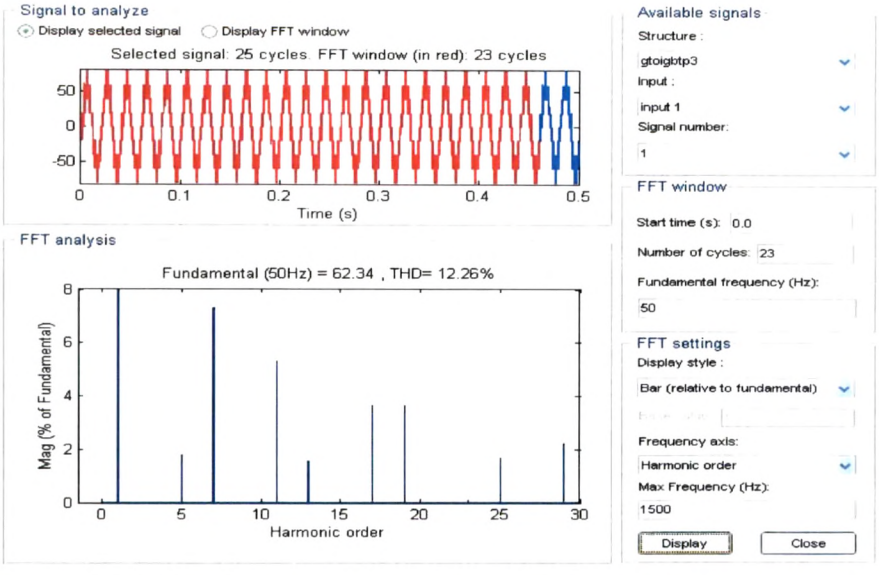

Fig. 4.31 FFT analysis and THD for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique for equal DC sources

B) Unequal DC sources

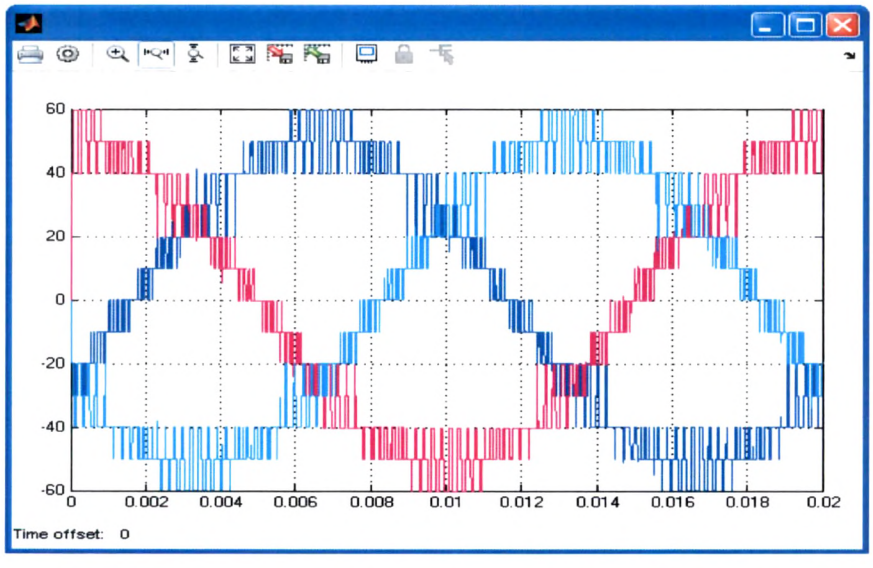

Fig. 4.32 Simulink output for three phase asymmetric hybrid multilevel inverter hybrid modulation technique with unequal DC sources

Three phase asymmetric hybrid multilevel inverter with unequal DC sources with hybrid modulation technique output is shown in Fig. 4.32 with DC sources as 10V for

IGBT bridges and 20V for GTO bridges. Control signals are phase shifted by 120^0. As DC voltages sources are unequal output is thirteen level as shown in Fig. 4.33. Fig. 4.34 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

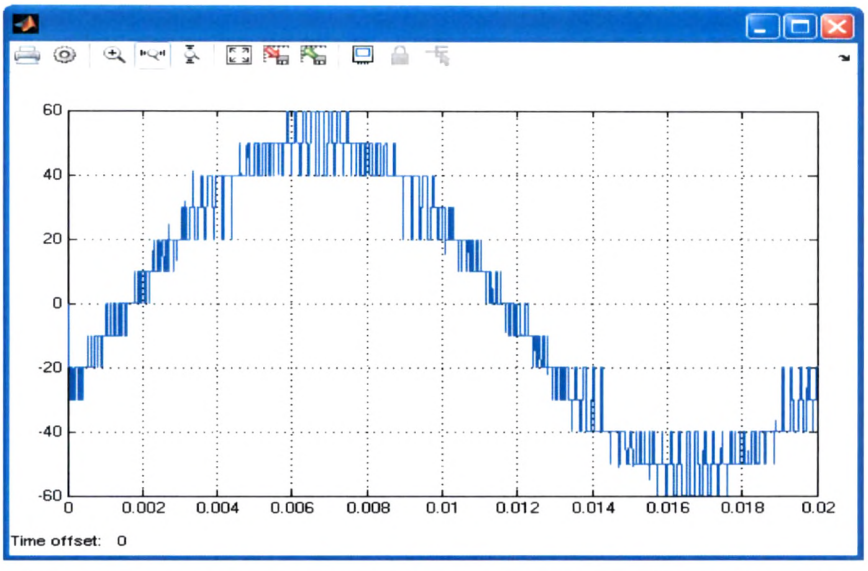

Fig. 4.33 One phase output from three phase asymmetric hybrid multilevel inverter hybrid modulation technique with unequal DC sources

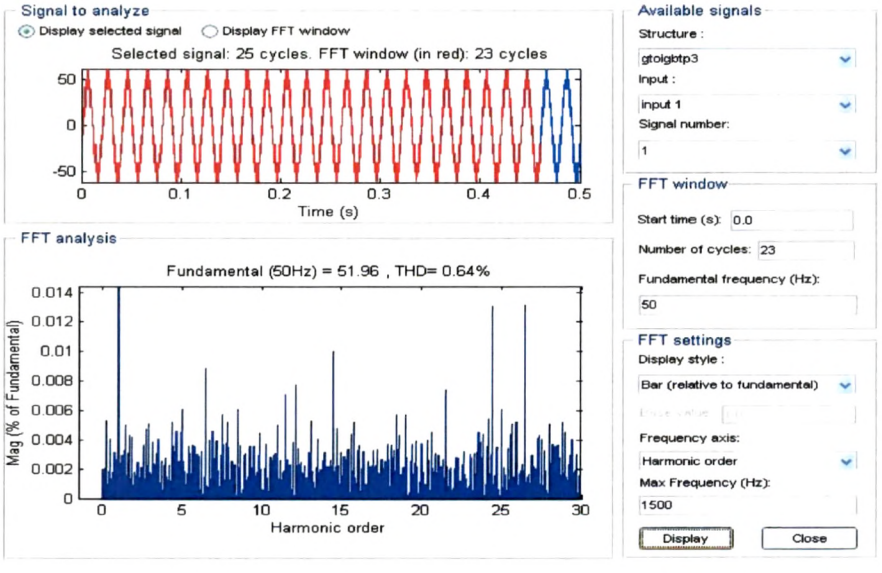

Fig. 4.34 FFT analysis and THD for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique for unequal DC sources

4.2.2 SYMMETRICAL HYBRID MULTILEVEL INVERTER

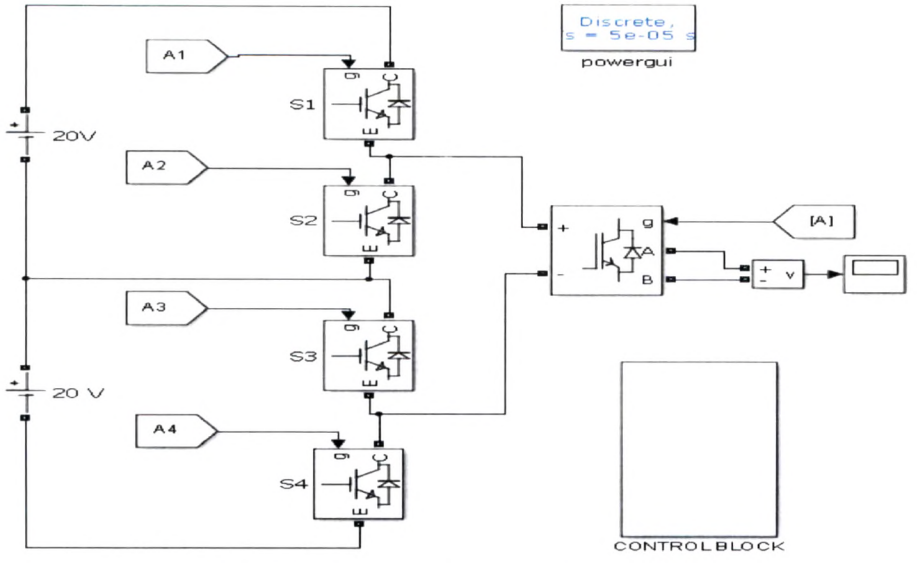

Fig. 4.35 Simulink block for five level symmetric hybrid multilevel inverter

Block diagram structure for symmetrical hybrid multilevel inverter is shown in Fig. 4.35.DC voltage sources are equal. As per switching pattern discussed in chapter 2 simulations are done. Control block is already shown in previous

4.2.2.1 Symmetrical Hybrid Multilevel Inverter with Staircase Technique

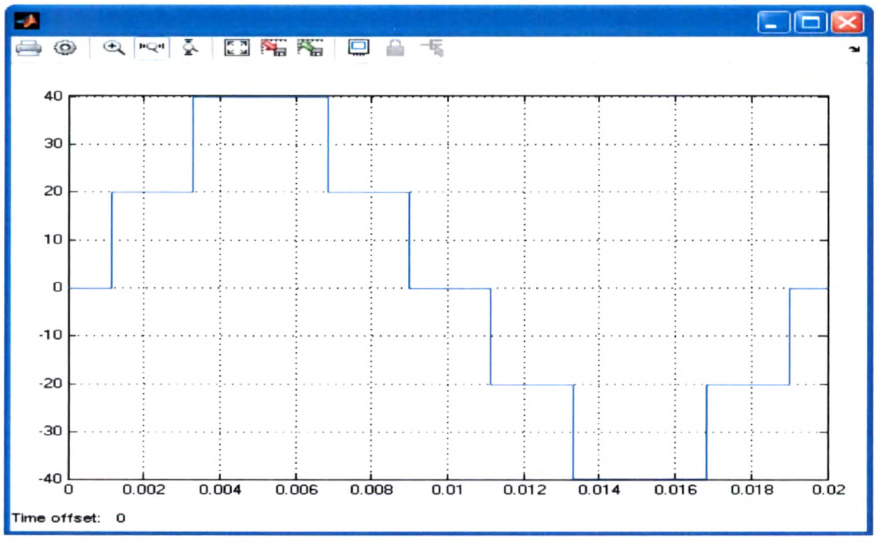

Fig. 4.36 Simulink output for five level symmetric multilevel inverter

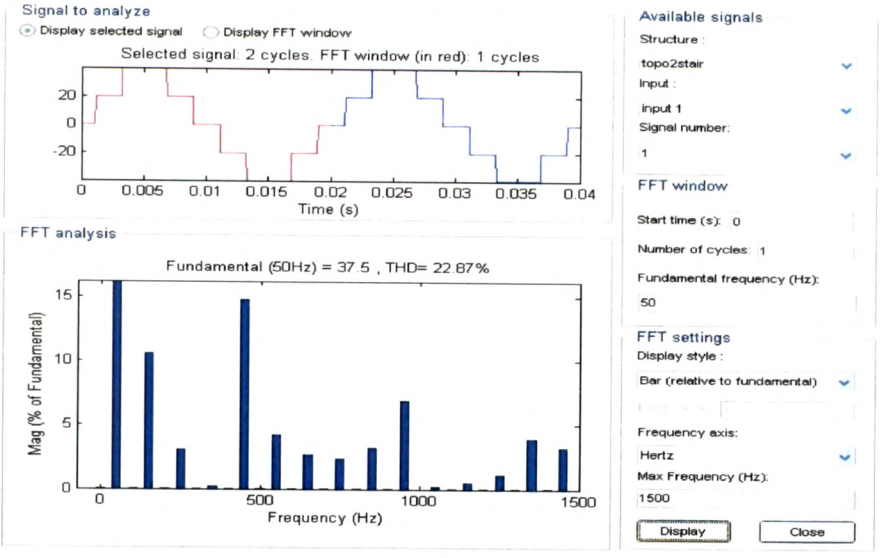

Fig. 4.37 FFT analysis and THD for single phase symmetrical hybrid multilevel inverter with staircase technique

In symmetrical hybrid multilevel inverter switches are switched at approximately 20^0 and 58^0 to obtain 5 level output as shown in Fig. 4.36. To optimize output with different switching angles can be applied and accordingly THD changes. Fig. 4.37 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency.

4.2.2.2 Single Phase Symmetrical Hybrid Multilevel Inverter with Phase Shift Modulation Technique

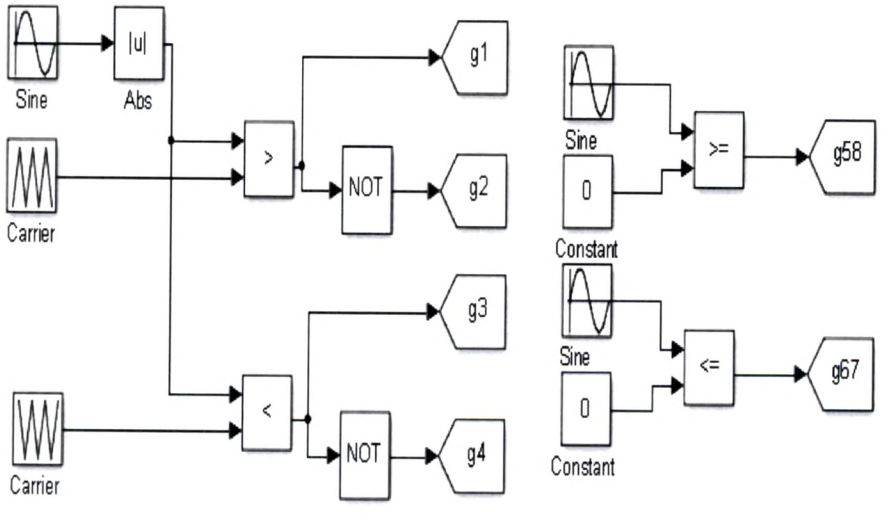

Fig. 4.38 Control block for single phase symmetrical hybrid multilevel inverter with phase shift modulation technique

Fig. 4.38 control block for single phase symmetrical hybrid multilevel inverter with phase shift modulation technique. Fig. 4.39 shows carrier and modulating signal for PS technique for single phase symmetrical hybrid multilevel inverter.

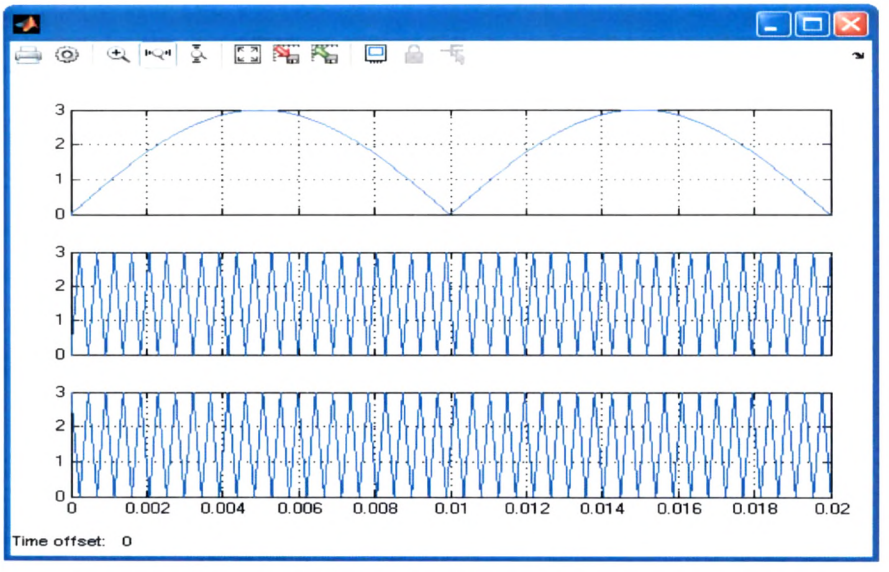

Fig. 4.39 Carrier and modulating signal for symmetrical hybrid MLI with PS technique

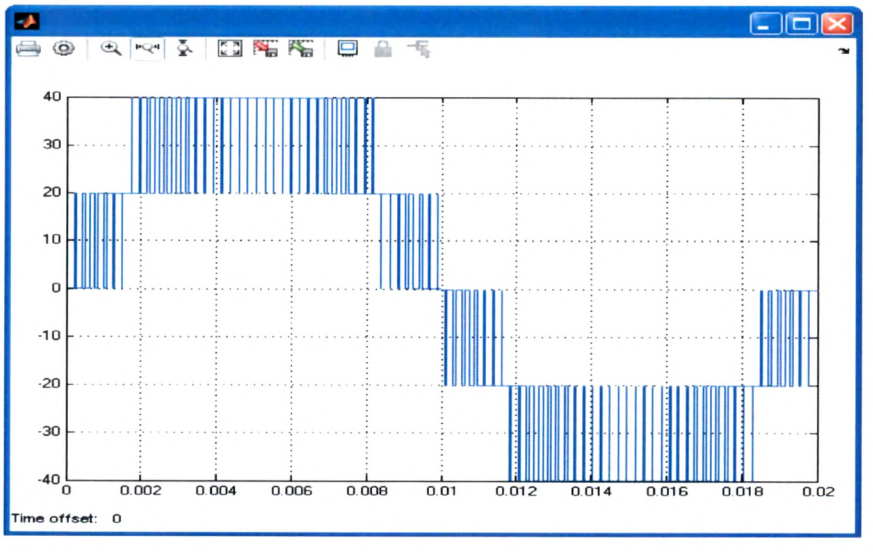

Fig. 4.40 Single phase output for symmetrical multilevel inverter for PS modulation

Fig. 4.40 shows 5 level output voltage where each source is 20V and phase shift modulation technique is applied. Frequency modulation index is approximately 43. Thus output can be changed with different modulation index for amplitude and frequency

hence THD will change accordingly. Fig. 4.41 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

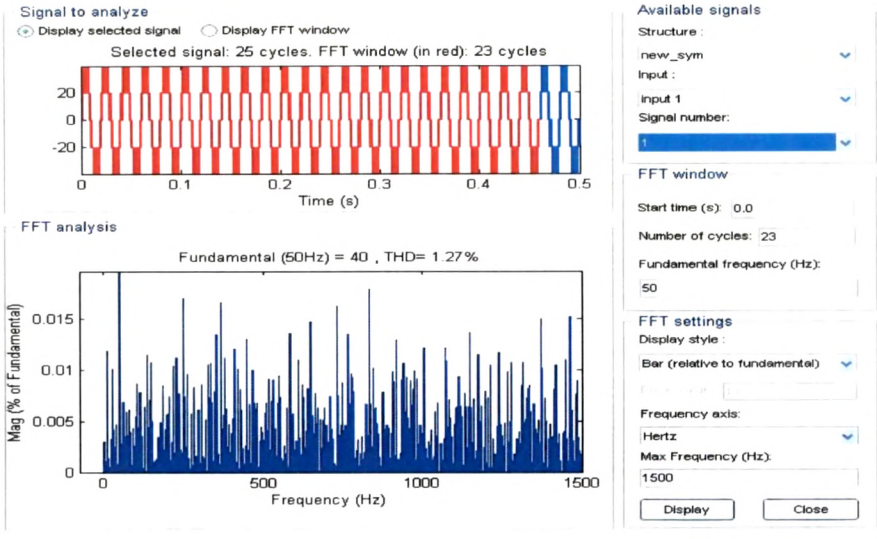

Fig. 4.41 FFT analysis and THD for single phase symmetrical hybrid multilevel inverter with PS modulation

4.2.2.3 Three Phase Symmetrical Hybrid Multilevel Inverter with Phase Shift Modulation Technique

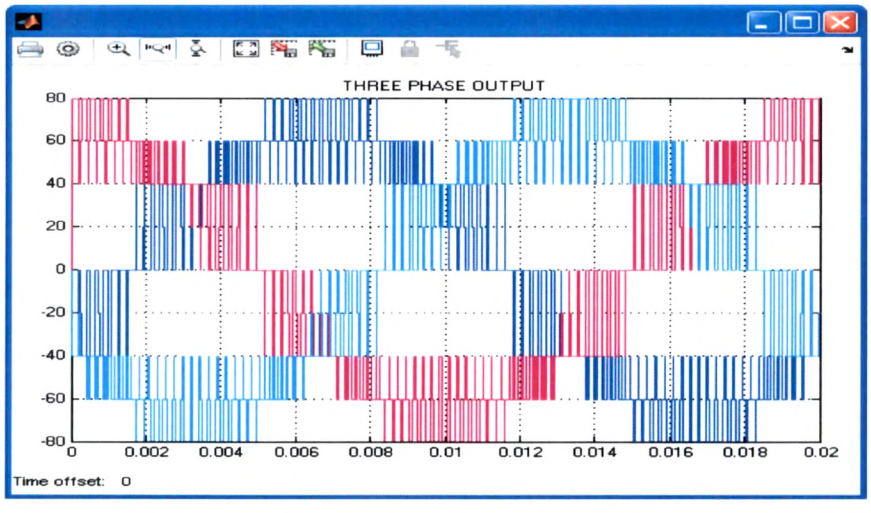

Fig. 4.42 Three phase output for symmetric multilevel inverter for PS modulation

Output for three phase symmetric hybrid multilevel inverter is shown in Fig. 4.42 with DC sources as 20V. Control signals are phase shifted by 120^0. Fig. 4.43 shows nine level output for single leg of three phase symmetric hybrid multilevel inverter. Fig. 4.44

corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

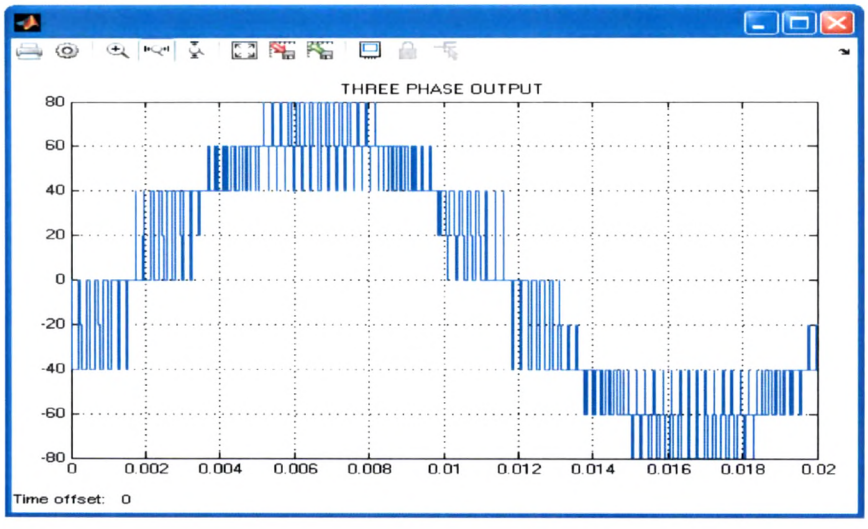

Fig. 4.43 One phase output from three phase symmetric hybrid multilevel inverter PS modulation technique

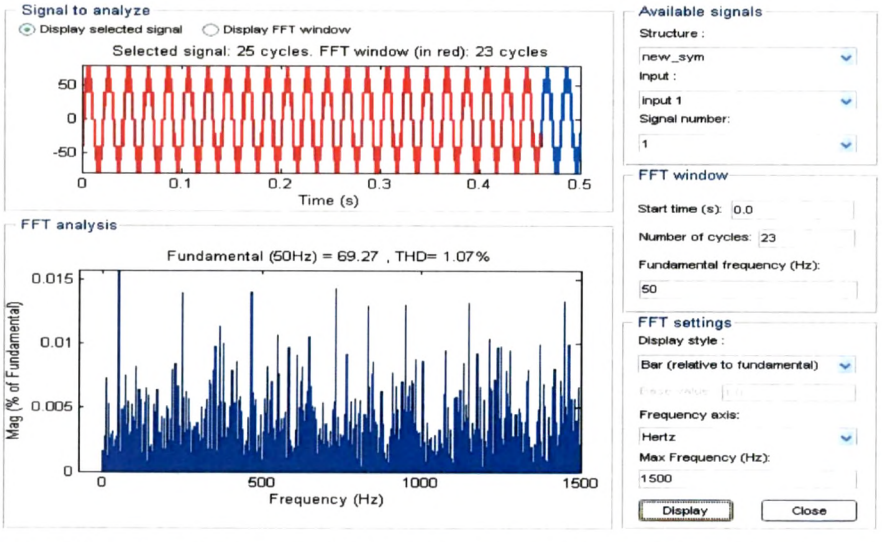

Fig. 4.44 FFT analysis and THD for three phase symmetric hybrid multilevel inverter with PS modulation technique

4.2.3 HALF BRIDGE MODULES BASED HYBRID MULTILEVEL INVERTER

Block diagram structure for single phase half bridge module based hybrid multilevel inverter is shown in Fig. 4.45. DC voltage sources are equal. In this topology half bridges are connected as shown and as per connection output is asymmetric four level output with positive levels greater than negative levels. Hence as shown in Fig.4.45

constant is added to obtain symmetric output across zero level [Fig. 4.4].

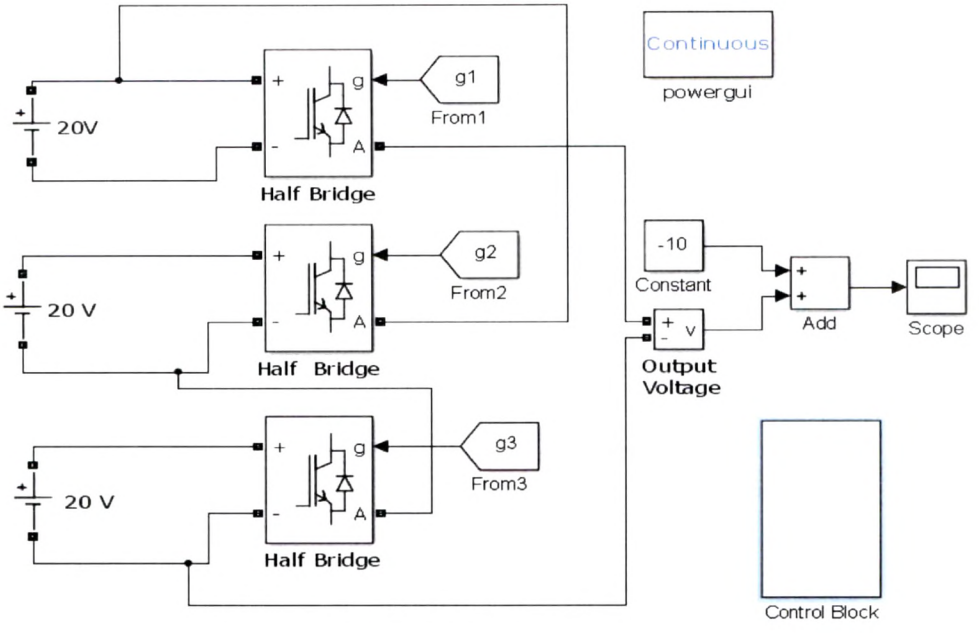

Fig. 4.45 Simulink block for half bridge module based hybrid multilevel inverter

4.2.3.1 Single Phase Half Bridge Modules Based Hybrid Multilevel Inverter with Phase Disposition Modulation Technique

Fig. 4.46 shows carrier and modulating signal for PD technique for single phase half bridge modules based hybrid multilevel inverter.

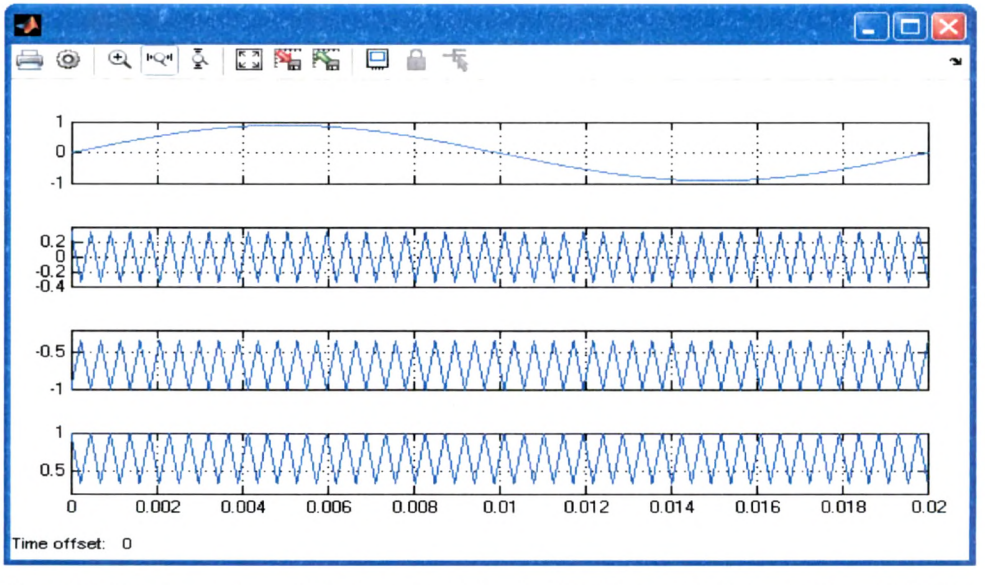

Fig. 4.46 Carrier and modulating signal for half bridge module based hybrid MLI with PD technique

Fig. 4.47 shows 4 level output voltage where each source is 20V and phase disposition modulation technique is applied. Frequency modulation index is approximately 43. Thus output can be changed with different modulation index for amplitude and frequency hence THD will change accordingly. Fig. 4.48 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

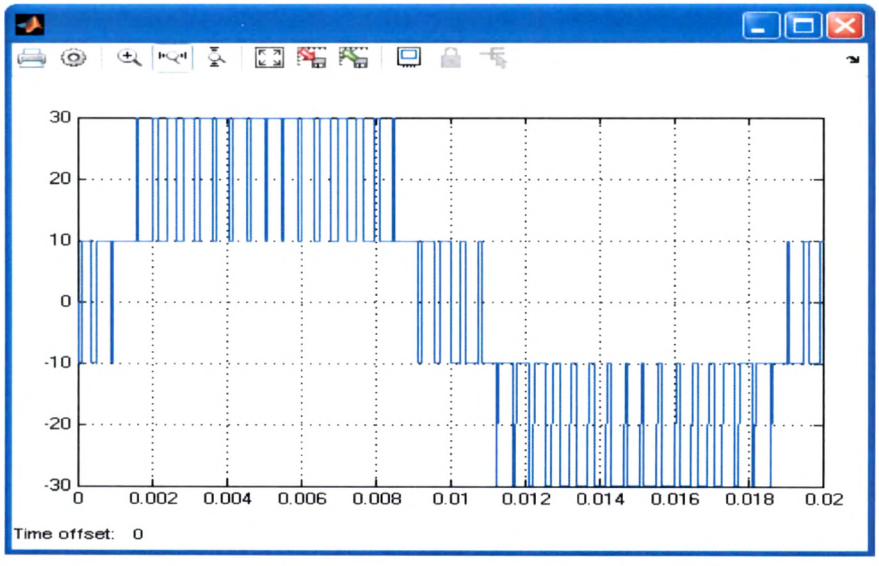

Fig. 4.47 Single phase output for half bridge modules based hybrid multilevel inverter for PD modulation

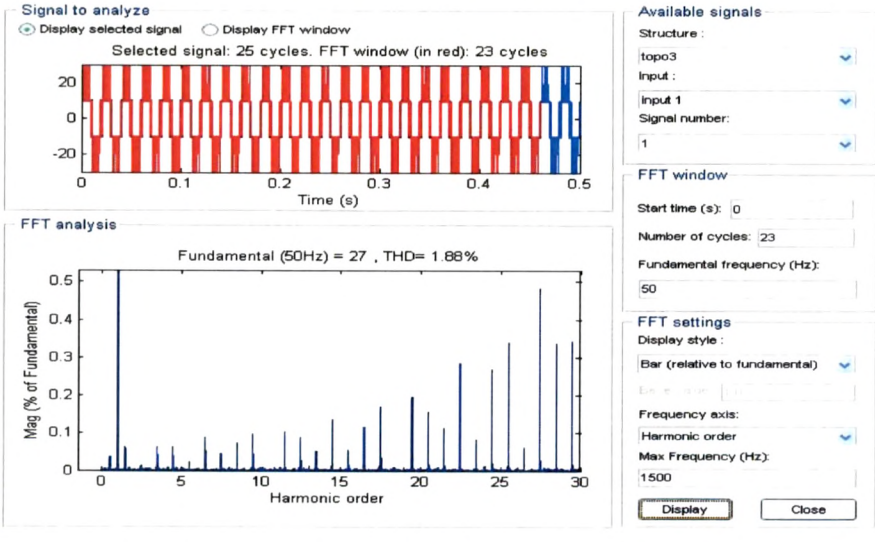

Fig. 4.48 FFT analysis and THD for single phase half bridge module based hybrid multilevel inverter with PD modulation

4.2.3.2 Three Phase Half Bridge Module Based Hybrid Multilevel Inverter with Phase Disposition Modulation Technique

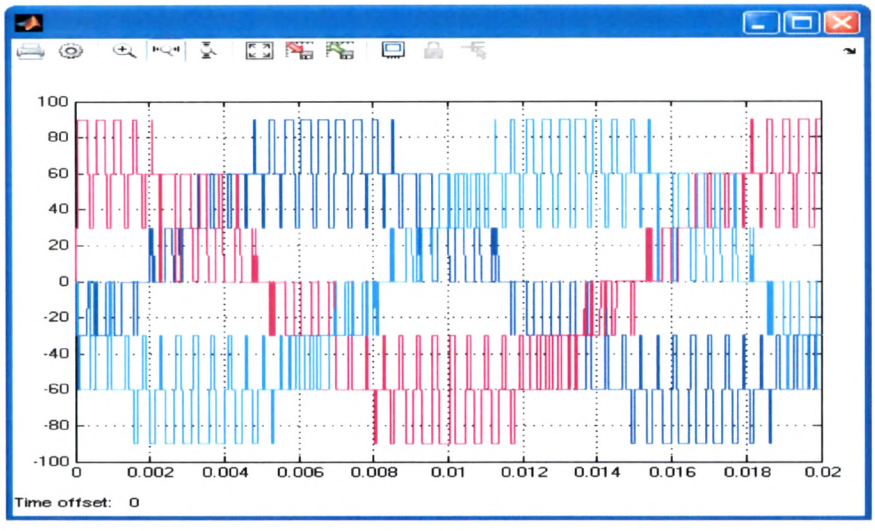

Fig. 4.49 Three phase output for half bridge module based multilevel inverter for PD modulation

Output for three phase half bridge module based hybrid multilevel inverter is shown in Fig. 4.49 with DC sources as 30V. Control signals are phase shifted by 120^0.

Fig. 4.50 shows seven level output for single leg of three phase symmetric hybrid multilevel inverter. Fig. 4.51 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

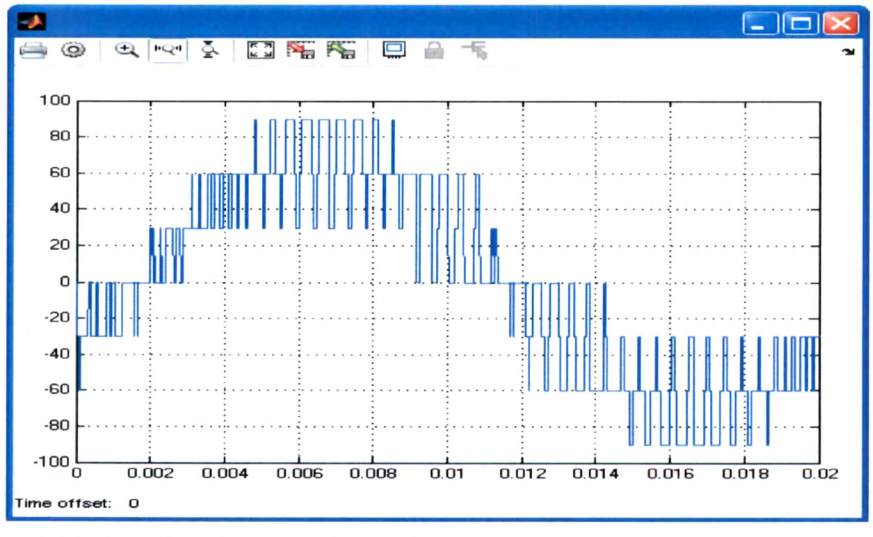

Fig. 4.50 One phase output from three phase half bridge module based hybrid multilevel inverter PD modulation technique

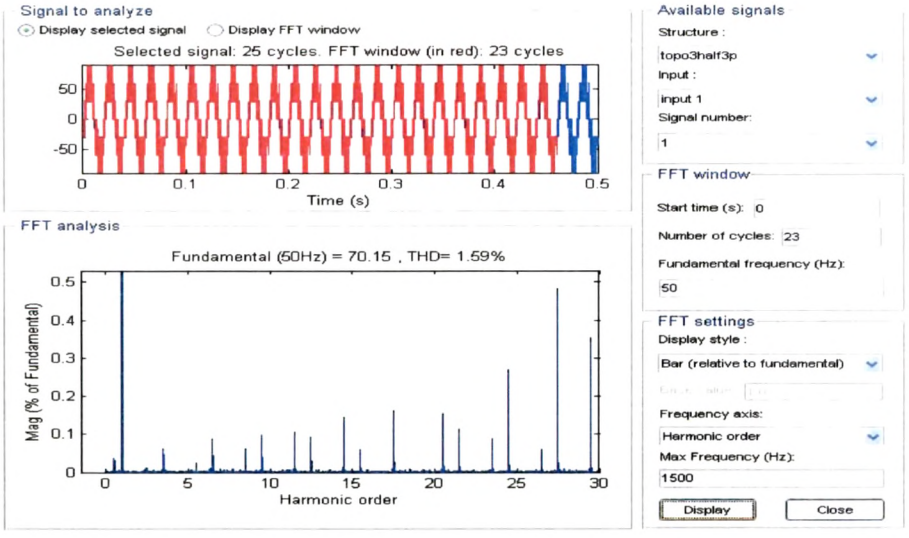

Fig. 4.51 FFT analysis and THD for three phase half bridge module based hybrid multilevel inverter with PD modulation technique

Table 4.1 MATLAB simulation summary

Topology	Phase	Modulation Technique	Output Levels	THD %
Cascaded multilevel inverter	1	--	5	21.92
	1	PD	5	1.31
	1	--	7	9.51
	1	PD	7	0.93
	1	--	9	5.3
Asymmetric hybrid multilevel inverter	1	HYBRID	5	0.8
	1	PD	5	1.17
	3	HYBRID	9	0.64
Symmetrical hybrid multilevel inverter	1	PS	5	1.27
	3	PS	9	1.07
Half bridge modules based hybrid multilevel inverter	1	PD	4	1.88
	3	PD	7	1.59

4.3 SUMMARY

Different MATLAB simulations are done for cascaded multilevel inverter and hybrid multilevel inverter. Comparison is done on basis of THD. Results are summarized in Table 4.1. It is observed that for particular modulation index THD does not vary much with change in modulation technique. Number of stages, number of switches, number of sources, number of capacitors, overall cost etc. are the selection criteria for given application.