

LIST OF FIGURES

Fig. 2.1	Single leg of multilevel inverter (a) Two level (b) Three level (c) m level	10
Fig. 2.2	Three level diode clamped inverter	10
Fig. 2.3	Five level diode clamped inverter	12
Fig. 2.4	Three level flying capacitor multilevel inverter	13
Fig. 2.5	Five level flying capacitor multilevel inverter	13
Fig. 2.6	Five level cascaded multilevel inverter	15
Fig. 2.7	Asymmetric hybrid multilevel inverter (a) seven level (b) nine level	18
Fig. 2.8	Hybrid multilevel inverter based on half-bridge modules	20
Fig. 2.9	New symmetrical hybrid multilevel inverter	22
Fig. 2.10	Output voltage waveform for new symmetrical hybrid multilevel inverter	22
Fig. 2.11	Hybrid clamped five level inverter	23
Fig. 2.12	Distinct series connected cells hybrid multilevel inverter	25
Fig. 2.13	Hybrid medium voltage inverter based on NPC inverter	26
Fig. 2.14	Hybrid multilevel inverter based on main inverter and conditioning inverter	28
Fig. 2.15	New hybrid asymmetrical multilevel inverter	29
Fig. 2.16	Three phase hybrid multilevel inverter with single DC source	30
Fig. 2.17	Single phase hybrid multilevel inverter with single DC source	31
Fig. 2.18	Output voltage for single phase hybrid multilevel inverter with single DC source	32
Fig. 2.19	Capacitor voltage regulation	32
Fig. 3.1	Block diagram for novel modulation techniques	35
Fig. 3.2	Classification for multicarrier pulse width modulation	36
Fig. 3.3	Cascaded H-bridge inverter (a) symmetric five level (b) Asymmetric seven level	37
Fig. 3.4	(a) Phase Disposition technique (b) Five level inverter output voltage	38
Fig. 3.5	(a) Phase Opposition Disposition technique (b) Five level inverter output voltage	38
Fig. 3.6	Alternative Phase Opposition Disposition technique (b) Five level inverter Output Voltage	39
Fig. 3.7	(a) Phase Shifted Technique (b) Five level inverter Output Voltage	40
Fig. 3.8	Hybrid modulation strategy	42

Fig. 3.9	High power cell switching	42
Fig. 3.10	Low power cell switching	42
Fig. 3.11	Output phase voltage	43
Fig. 3.12	(a) Inverted sine technique (b) Five level inverter output voltage	43
Fig. 3.13	(a) Variable Frequency Inverted Sine Carrier (b) Five level inverter output voltage	44
Fig. 3.14	Low and high frequency PDPWM	46
Fig. 3.15	Optimized hybrid PDPWM switching pattern for five level cascaded MLI	46
Fig. 3.16	Analog circuit to make the reference signals in SFO-PWM technique	47
Fig. 3.17	SFO-PWM technique for a 9-level asymmetric inverter output	48
Fig. 3.18	PSC-SFO PWM modulating signal generation	48
Fig. 3.19	Phase shifted carrier switching frequency optimal pulse width modulation	49
Fig. 3.20	Hybrid clamped five level inverter	50
Fig. 3.21	Carrier waveforms of the upper four main switching devices for a hybrid-clamped five-level inverter with the PDPWM technique. (a) Carrier of Sa1. (b) Carrier of Sa2. (c) Carrier of Sa3. (d) Carrier of Sa4	51
Fig. 3.22	Device switching on or off (a) Higher carrier cells and lower carrier cells in phase. (b) Higher carrier cells and lower carrier cells in phase opposition	52
Fig. 3.23	PWM pulse waveforms respectively produced by the carrier cells in phase opposition intersecting a certain modulation wave	52
Fig. 3.24	Carrier waveforms of the upper six main switching devices for a seven level inverter with the HLCCAPOPWM technique. (a) Carrier of Sa1. (b) Carrier of Sa2. (c) Carrier of Sa3. (d) Carrier of Sa4. (e) Carrier of Sa5. (f) Carrier of Sa6	52
Fig. 3.25	Carrier waveforms and the representative PWM pulse waveforms of the “W” PDPWM technique	53
Fig. 3.26	Carrier waveforms and the representative PWM pulse waveforms of the “M” PDPWM technique	54
Fig. 3.27	Carrier waveforms and the representative PWM pulse waveforms of AHPWM technique	54
Fig. 3.28	Space vector diagram for the two-level inverter	56
Fig. 3.29	\vec{V}_{ref} synthesized by \vec{V}_1 , \vec{V}_2 and \vec{V}_0	58
Fig. 3.30	Seven-segment switching sequence for \vec{V}_{ref} in sector I	58
Fig. 3.31	Eight switching state topologies of a voltage source inverter	59

Fig. 3.32	Three-level NPC inverter	59
Fig. 3.33	Output voltage waveforms of the NPC inverter	59
Fig. 4.1	Simulink block for cascaded multilevel inverter	63
Fig. 4.2	Simulink output for five level cascaded multilevel inverter	64
Fig. 4.3	FFT analysis and THD for five level cascaded multilevel inverter	64
Fig. 4.4	Control block for five level cascaded MLI with PD technique	65
Fig. 4.5	Carrier and modulating signal for five level cascaded MLI with PD technique	66
Fig. 4.6	Simulink output for five level cascaded multilevel inverter with PD technique	66
Fig. 4.7	FFT analysis and THD for five level cascaded multilevel inverter with PD technique	67
Fig. 4.8	Simulink output for seven level CMLI using three H bridges	67
Fig. 4.9	FFT analysis and THD for seven level CMLI for specified angles	68
Fig. 4.10	Simulink output for 7 level CMLI using 2 H bridges	68
Fig. 4.11	FFT analysis and THD for 7 level CMLI for specified angles	69
Fig. 4.12	Simulink output for 7 level CMLI with PD technique	70
Fig. 4.13	FFT analysis and THD for seven level cascaded multilevel inverter with PD technique	70
Fig. 4.14	Simulink output for 7 level CMLI with POD technique	71
Fig. 4.15	Simulink output for 7 level CMLI with APOD technique	71
Fig. 4.16	Simulink output for 9 level CMLI for 4 H bridges	72
Fig. 4.17	FFT analysis and THD for 9 level CMLI for specified angles	72
Fig. 4.18	Simulink output for nine level cascaded multilevel inverter for 2 H bridges	73
Fig. 4.19	FFT analysis and THD for 9 level CMLI for specified angles	73
Fig. 4.20	Simulink block for single phase asymmetric hybrid multilevel inverter	74
Fig. 4.21	Control block for single phase asymmetric hybrid multilevel inverter with hybrid modulation technique	75
Fig. 4.22	Control signals for asymmetric hybrid multilevel inverter	75
Fig. 4.23	Simulink output for single phase asymmetric multilevel inverter with hybrid modulation technique for equal DC sources	76
Fig. 4.24	FFT analysis and THD for asymmetric hybrid multilevel inverter with hybrid modulation technique for equal DC sources	76
Fig. 4.25	Simulink output for single phase asymmetric multilevel inverter with hybrid modulation technique for unequal DC sources	77
Fig. 4.26	FFT analysis and THD for asymmetric hybrid multilevel inverter	77

	with hybrid modulation technique for unequal DC sources	
Fig. 4.27	Simulink output for single phase asymmetric multilevel inverter with PD technique for equal voltages	78
Fig. 4.28	FFT analysis and THD for asymmetric hybrid multilevel inverter with PD modulation technique for equal DC sources	78
Fig. 4.29	Simulink output for three phase asymmetric hybrid multilevel inverter hybrid modulation technique with equal voltages	79
Fig. 4.30	One phase output from three phase asymmetric hybrid multilevel inverter hybrid modulation technique with equal voltages	79
Fig. 4.31	FFT analysis and THD for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique for equal DC sources	80
Fig. 4.32	Simulink output for three phase asymmetric hybrid multilevel inverter hybrid modulation technique with unequal DC sources	80
Fig. 4.33	One phase output from three phase asymmetric hybrid multilevel inverter hybrid modulation technique with unequal DC sources	81
Fig. 4.34	FFT analysis and THD for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique for unequal DC sources	81
Fig. 4.35	Simulink block for five level symmetric hybrid multilevel inverter	82
Fig. 4.36	Simulink output for five level symmetric multilevel inverter	82
Fig. 4.37	FFT analysis and THD for single phase symmetrical hybrid multilevel inverter with staircase technique	83
Fig. 4.38	Control block for single phase symmetrical hybrid multilevel inverter with phase shift modulation technique	83
Fig. 4.39	Carrier and modulating signal for symmetrical hybrid MLI with PS technique	84
Fig. 4.40	Single phase output for symmetrical multilevel inverter for PS modulation	84
Fig. 4.41	FFT analysis and THD for single phase symmetrical hybrid multilevel inverter with PS modulation	85
Fig. 4.42	Three phase output for symmetric multilevel inverter for PS modulation	85
Fig. 4.43	One phase output from three phase symmetric hybrid multilevel inverter PS modulation technique	86
Fig. 4.44	FFT analysis and THD for three phase symmetric hybrid multilevel inverter with PS modulation technique	86
Fig. 4.45	Simulink block for half bridge module based multilevel inverter	87
Fig. 4.46	Carrier and modulating signal for half bridge module based hybrid MLI with PD technique	87
Fig. 4.47	Single phase output for half bridge modules based hybrid	88

	multilevel inverter for PD modulation	
Fig. 4.48	FFT analysis and THD for single phase half bridge module based hybrid multilevel inverter with PD modulation	88
Fig. 4.49	Three phase output for half bridge module based multilevel inverter for PD modulation	89
Fig. 4.50	One phase output from three phase half bridge module based hybrid multilevel inverter PD modulation technique	89
Fig. 4.51	FFT analysis and THD for three phase half bridge module based hybrid multilevel inverter with PD modulation technique	90
Fig. 5.1	Simulink block for single phase HMLI	92
Fig. 5.2	Simulink output for single phase HMLI with PD modulation technique	93
Fig. 5.3	FFT analysis and THD for single phase HMLI with PD modulation technique	93
Fig. 5.4	Simulink output for single phase HMLI with POD modulation technique	94
Fig. 5.5	FFT analysis and THD for single phase HMLI with POD modulation technique	94
Fig. 5.6	Simulink output for single phase HMLI with APOD modulation technique	95
Fig. 5.7	FFT analysis and THD for single phase HMLI with APOD modulation technique	95
Fig. 5.8	Simulink output for single phase HMLI with PS modulation technique	96
Fig. 5.9	FFT analysis and THD for single phase HMLI with PS modulation technique	96
Fig. 5.10	Simulink output for single phase HMLI with hybrid modulation technique	97
Fig. 5.11	FFT analysis and THD for single phase HMLI with hybrid modulation technique	97
Fig. 5.12	Control block for HMLI with third harmonic injection modulation technique	98
Fig. 5.13	Simulink output for single phase HMLI with third harmonic injection modulation technique	98
Fig. 5.14	FFT analysis and THD for single phase HMLI with third harmonic injection modulation technique	99
Fig. 5.15	Control block for HMLI with ISPWM technique	99
Fig. 5.16	Simulink output for single phase HMLI with inverted sine modulation technique	100
Fig. 5.17	FFT analysis and THD for single phase HMLI with inverted sine	100

	modulation technique	
Fig. 5.18	Simulink block for three phase HMLI	101
Fig. 5.19	Simulink output for three phase HMLI with PD modulation technique	101
Fig. 5.20	One phase output from three phase HMLI PD modulation technique	102
Fig. 5.21	FFT analysis and THD for HMLI with PD modulation technique	102
Fig. 5.22	Simulink output for three phase HMLI with POD modulation technique	103
Fig. 5.23	One phase output from three phase HMLI POD modulation technique	103
Fig. 5.24	FFT analysis and THD for HMLI with POD modulation technique	104
Fig. 5.25	Simulink output for three phase HMLI with APOD modulation technique	104
Fig. 5.26	One phase output from three phase HMLI APOD modulation technique	105
Fig. 5.27	FFT analysis and THD for HMLI with APOD modulation technique	105
Fig. 5.28	Simulink output for three phase HMLI with PS modulation technique	106
Fig. 5.29	One phase output from three phase HMLI PS modulation technique	106
Fig. 5.30	FFT analysis and THD for HMLI with PS modulation technique	107
Fig. 5.31	Simulink output for three phase HMLI with hybrid modulation technique	107
Fig. 5.32	One phase output from three phase HMLI hybrid modulation technique	108
Fig. 5.33	FFT analysis and THD for HMLI with hybrid modulation technique	108
Fig. 5.34	Simulink output for three phase HMLI with third harmonic injection modulation technique	109
Fig. 5.35	One phase output from three phase HMLI third harmonic injection modulation technique	109
Fig. 5.36	FFT analysis and THD for HMLI with third harmonic injection modulation technique	110
Fig. 6.1	EPB 28335 with peripherals	114
Fig. 6.2	CCS setup	115
Fig. 6.3	Emulator selection	115
Fig. 6.4	MATLAB SIMULINK model for control signals	116

Fig. 6.5	Building model in MATLAB SIMULINK	116
Fig. 6.6	Project built in CCS	117
Fig. 6.7	Control circuit for generating gating signals	118
Fig. 7.1	Three phase hybrid multilevel inverter circuit diagram	120
Fig. 7.2	Single leg of hybrid multilevel inverter circuit diagram	121
Fig. 7.3	Regulated power supply	123
Fig. 8.1	Control signals for single phase HMLI without modulation	126
Fig. 8.2	Five level output for single phase HMLI without modulation	127
Fig. 8.3	FFT analysis and THD for single phase HMLI without modulation	127
Fig. 8.4	Control signals for single phase HMLI with PD modulation technique	128
Fig. 8.5	Single phase HMLI output with PD modulation technique	129
Fig. 8.6	Current through RL load for single phase HMLI with PD modulation technique	129
Fig. 8.7	Single phase HMLI output and FFT with PD modulation technique for R load	129
Fig. 8.8	FFT analysis and THD for single phase HMLI with PD modulation technique	130
Fig. 8.9	Single phase HMLI output with PD modulation technique for R load	130
Fig. 8.10	Control signals for three phase HMLI with PD modulation technique	131
Fig. 8.11	Three phase HMLI output with PD modulation technique	131
Fig. 8.12	Three phase HMLI output with PD modulation technique	131
Fig. 8.13	Three phase HMLI output with PD modulation technique	132
Fig. 8.14	FFT analysis and THD for 3 phase HMLI with PD modulation technique	132
Fig. 8.15	Three phase HMLI output with PD modulation technique 330 Ω	133
Fig. 8.16	Three phase HMLI output with PD modulation technique 330 Ω	133
Fig. 8.17	FFT analysis and THD for three phase Line to line voltage for RY 330 Ω star load	134
Fig. 8.18	Three phase HMLI output with PD modulation technique 33 Ω	134
Fig. 8.19	Output voltage and current for Three phase HMLI with PD modulation	135
Fig. 8.20	Output current for three phase HMLI with PD modulation	135
Fig. 8.21	FFT analysis and THD for 3 phase HMLI with PD modulation technique	136
Fig. 8.22	Control signals for three phase HMLI with POD modulation	136

	technique	
Fig. 8.23	Three phase HMLI output voltage with POD modulation technique	137
Fig. 8.24	Three phase HMLI output with POD modulation technique	137
Fig. 8.25	Three phase HMLI output with POD modulation technique	137
Fig. 8.26	FFT analysis and THD for 3 phase HMLI with POD modulation technique	138
Fig. 8.27	Control signals for three phase HMLI with APOD modulation technique	138
Fig. 8.28	Three phase HMLI output with APOD modulation technique	139
Fig. 8.29	Three phase HMLI output with APOD modulation technique	139
Fig. 8.30	Three phase HMLI output with APOD modulation technique	139
Fig. 8.31	FFT analysis and THD for 3 phase HMLI with APOD modulation technique	140
Fig. 8.32	Control signals for three phase HMLI with third harmonic injection modulation technique	141
Fig. 8.33	Three phase HMLI output with third harmonic injection modulation technique	141
Fig. 8.34	Three phase HMLI output with third harmonic injection modulation technique	142
Fig. 8.35	Three phase HMLI output with third harmonic injection modulation technique	142
Fig. 8.36	FFT analysis and THD for 3 phase HMLI with third harmonic injection modulation technique Y-B	143
Fig. 8.37	Three phase HMLI output with third harmonic injection modulation technique	143
Fig. 8.38	Three phase HMLI output with third harmonic injection modulation technique	144
Fig. 8.39	Three phase HMLI output with third harmonic injection modulation technique	144
Fig. 8.40	FFT analysis and THD for 3 phase HMLI with third harmonic injection modulation technique	144
Fig. B.1	Hardware for control and power circuit	169
Fig. B.2	Buffer, optoisolator, driver and power switch	169
Fig. B.3	Panel for control and power circuit	170
Fig. B.4	Gating signals	170
Fig. B.5	Emulator and EPB28335	171
Fig. B.6	Hardware for regulated power supply	171
Fig. B.7	Panel for regulated power supply	172

Fig. B.8	Primary voltage selector	172
Fig. B.9	Setup for current measurement	173
Fig. B.10	Load	173
Fig. B.11	System setup	174
Fig. B.12	Emulator connected to CCS	174
Fig. B.13	Project built in CCS	175