Appendix C

Photo Gallery

Appendix C: Photo Gallery

The FTE Robot with wireless module is shown in Figure B. 1. The setup for Wireless Control of FTE Robot through remote computer is shown in Figure B. 2.

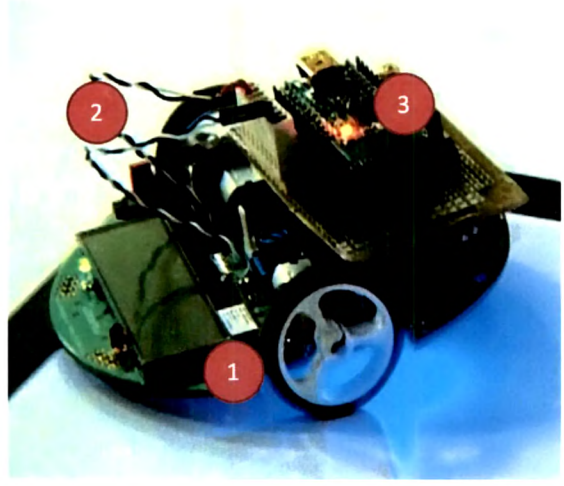

Figure B. 1: FTE Robot with Wireless module: 1)FTE Robot, 2)Connecting wires between Robot and Wireless Module and 3)Wireless Module.

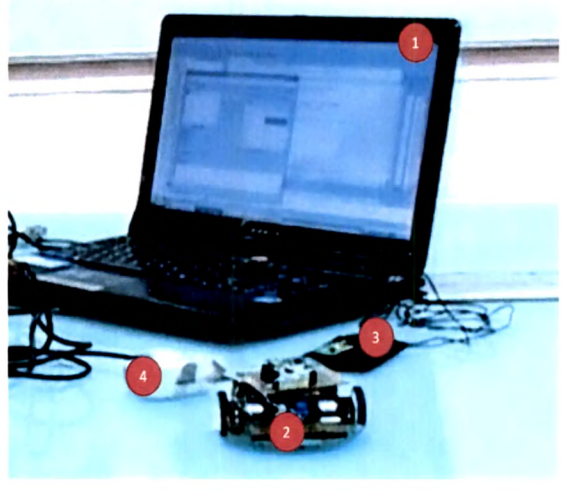

Figure B. 2: Wireless Control of FTE Robot setup: 1)Remote Computer, 2) FTE Robot with wireless module, 3) Transmitter Wireless Module, 4) JTAG Adapter Connector

The real-time implementation and testing of proposed algorithm for throughput optimization of LTE-A Downlink Physical Layer are done on TMS320C6713 DSK. The DSK is shown in Figure B. 3. Figure B. 4 shows the setup for real-time testing of algorithms in close-loop with MATLAB based LTE-A Link Level Simulator. Intel Core2Duo CPU 2.20GHz, 2.96 GB of RAM has installed MATLAB based LTE-A Link Level Simulator, CCS IDE and related toolbox useful for verification of algorithms.

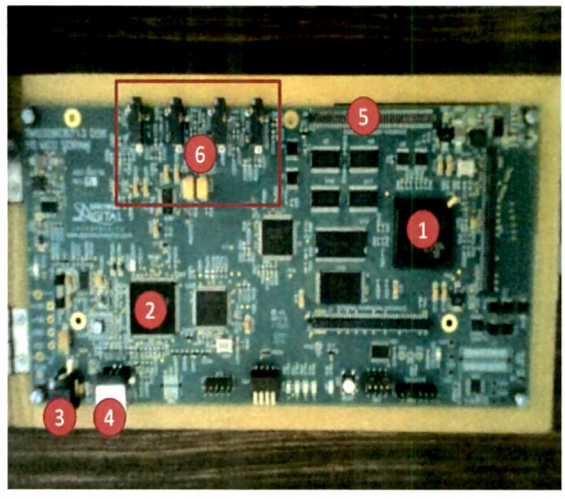

Figure B. 3: DSP Starter Kit: 1)TMS320C6713 DSP, 2)JTAG Emulation, 3)Power Jack, 4)USB Port, 5)Memory Expansion and 6)AIC23 Codec with peripherals

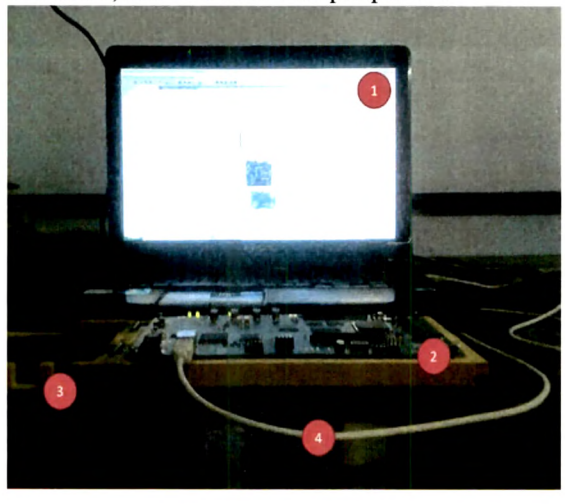

Figure B. 4: DSP Setup: 1)CPU Core2Duo with Software tools installed, 2)TMS320C6713 DSK, 3)Power Cable and 4)USB Cable

The real-time implementation and testing of proposed algorithm for throughput optimization of LTE-A Downlink Physical Layer are done on XUP Atlys Spartan-6 Development kit. The Atlys board is shown in Figure B. 5. Figure B. 6 shows the setup for real-time testing of algorithms in close-loop with MATLAB based LTE-A Link Level Simulator. Intel Core2Duo CPU 2.20GHz, 2.96 GB of RAM has installed MATLAB based LTE-A Link Level Simulator, Xilinx ISE Design Suite and related toolbox useful for verification of algorithms.

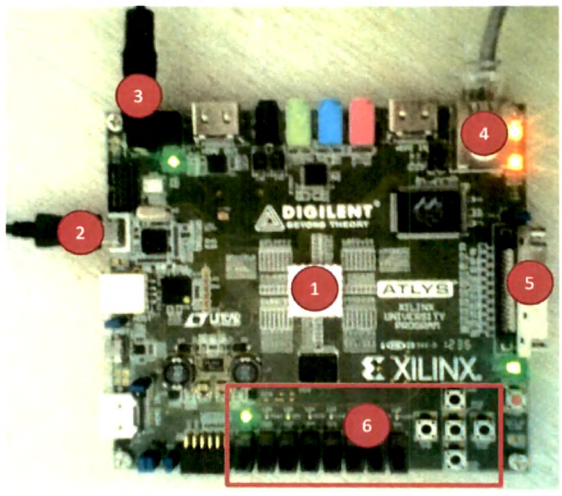

Figure B. 5: XUP Atlys Board: 1)Spartan-6 LX 45, 2)Adept USB Port, 3)Power Jack, 4)Ethernet connector, 5)VHDC connector and 6)LEDs, Slide Switches and Push buttons

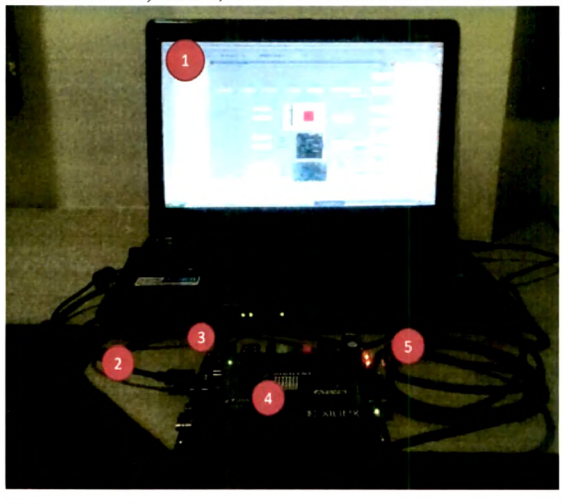

Figure B. 6: FPGA Setup: 1)CPU Core2Duo with Software tools installed, 2)USB cable, 3)Power cable, 4)Atlys board, 5)Gigabit Ethernet crossover cable