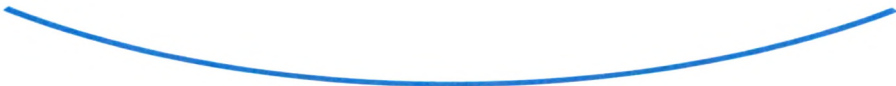




# Appendix A



# Development Environments



## A.1 Code Generation Using Xilinx ISE 14.6

### 1. Starting the ISE Design Suite

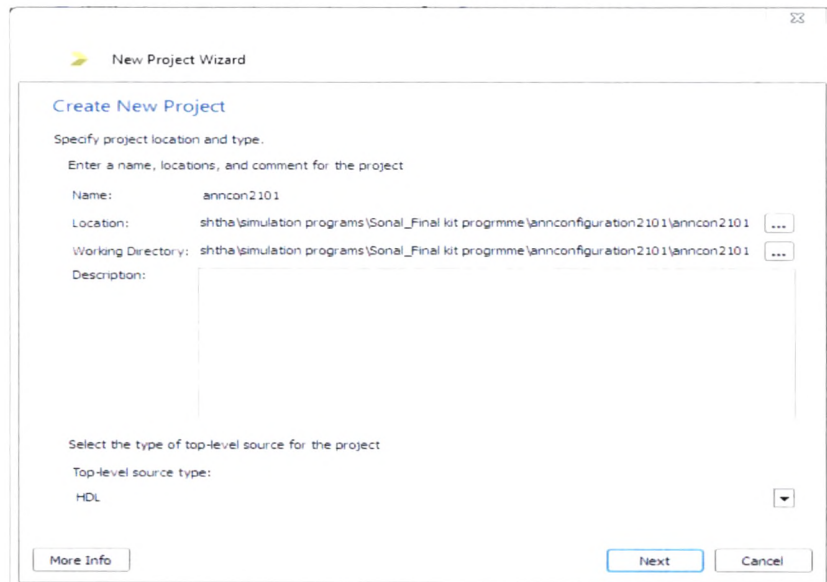
Follow these steps to launch Project Navigator software and create an ISE project.

1. To start the ISE Design Suite, double-click the Project Navigator icon (Figure A.1) on desktop as shown in Figure , or select **Start > All Programs > Xilinx ISE Design Suite > Xilinx Design Suite > ISE Design Tools > Project Navigator**.



**Figure A.1: Project Navigator Desktop Icon**

2. Click the New Project button to launch the New Project Wizard or from Project Navigator, select **File > New Project**. The New Project Wizard appears as shown in Figure A.2.



**Figure A.2: New Project Wizard—Create New Project Page**

3. Verify that HDL is selected as the Top-Level Source Type, and click Next. The New Project Wizard—Device Properties page appears as shown in Figure A.3.
4. In the window, select the device and project properties and change the settings according to FPGA board shown in Figure A.3.

- 5. Click **Next** and then **Finish**, to complete the project creation.

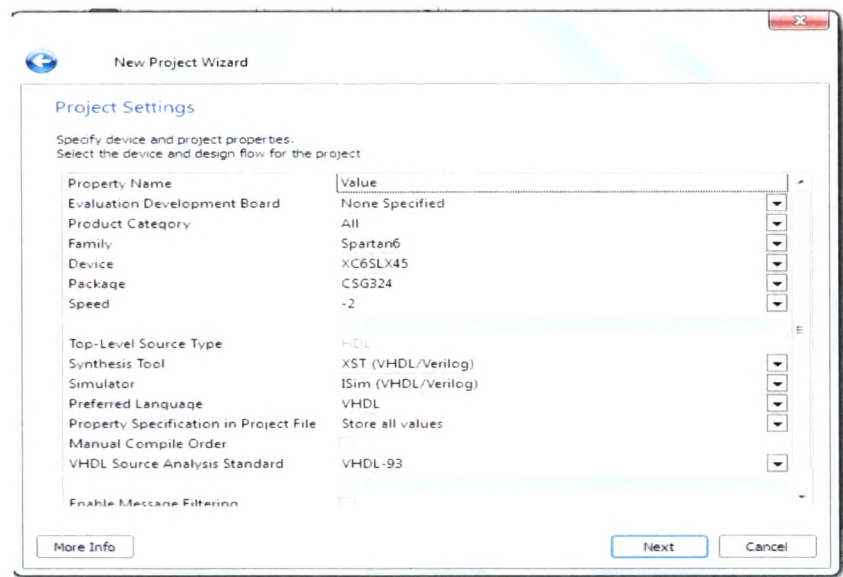


Figure A.3: New Project Wizard—Device Properties Page

2. Adding Source Files to the Project

- 1. Click the Add Source button in the Design Panel toolbar to select the sources provided for tutorial.
- 2. In the next window, make sure that the association and libraries have been properly specified for the tutorial sources. Compare setting with those in Figure A.4.
- 3. Click **OK**.

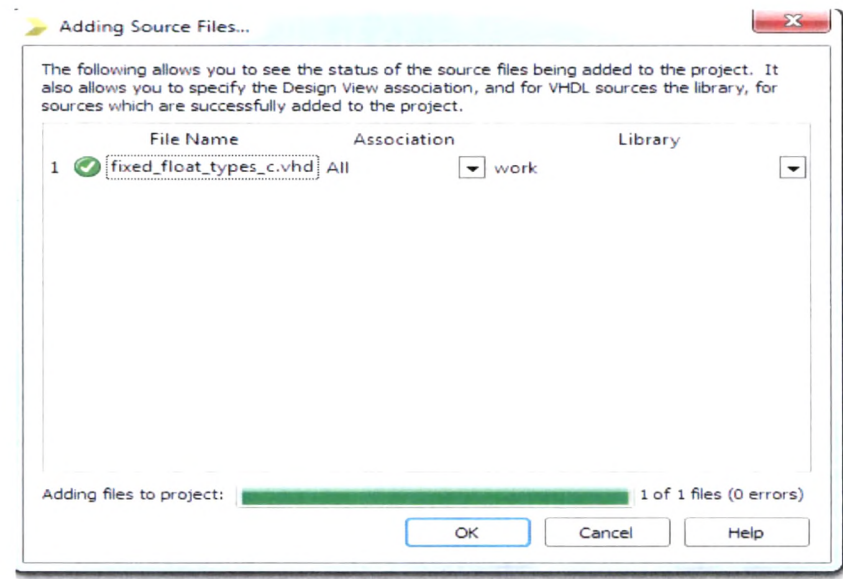


Figure A.4: Adding VHDL Test Bench

3. Launching a Behavioral Simulation

- 1. Now that the ISE project has been created for the tutorial design, we can proceed to set up and launch a behavioral simulation using ISim.

Setting Behavioral Simulation Properties

- ✖ To set behavioral simulation properties in ISE : In the Design Panel, select **Behavioral Simulation** from the dropdown list.
- ✖ We should now see the simulation processes available for the design in the Processes pane. (Refer to Figure A.5)
- 2. Right-click **Simulate Behavioral Model** under the ISim Simulator process and select **Properties**. The ISim Properties dialog box displays (Refer to Figure A.6).
- ✖ In this window we can set different simulation properties, such as simulation runtime, waveform database file location, and even a user-defined simulation command file to launch the simulation.
- ✖ For the purposes of this tutorial, we will disable the feature that runs the simulation for a specified amount of time.
- 3. In the ISim Properties dialog box, uncheck the property **Run for Specified Time**, and click **OK**.(Refer to Figure A.6)

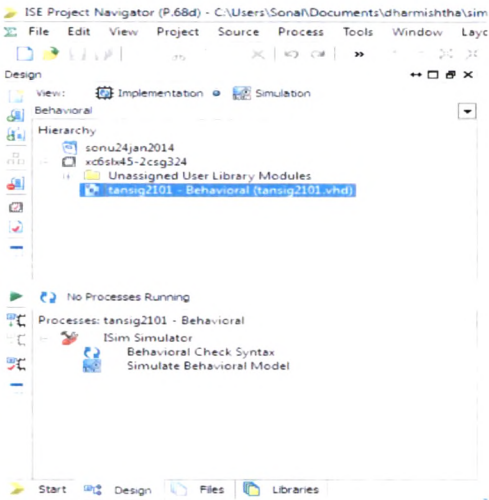


Figure A.5: Process Pane

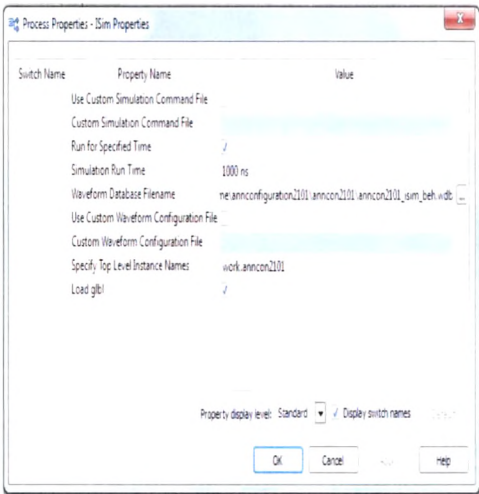


Figure A.6: ISim Properties Dialog Box

Now it is ready to launch the ISE Simulator to perform a behavioral simulation of the tutorial design. To launch the simulator:



In the Processes panel, double-click **Simulate Behavioral Model**. The ISim Graphical User Interface (GUI) (Figure A.7) will appear shortly after the design is successfully parsed and compiled.

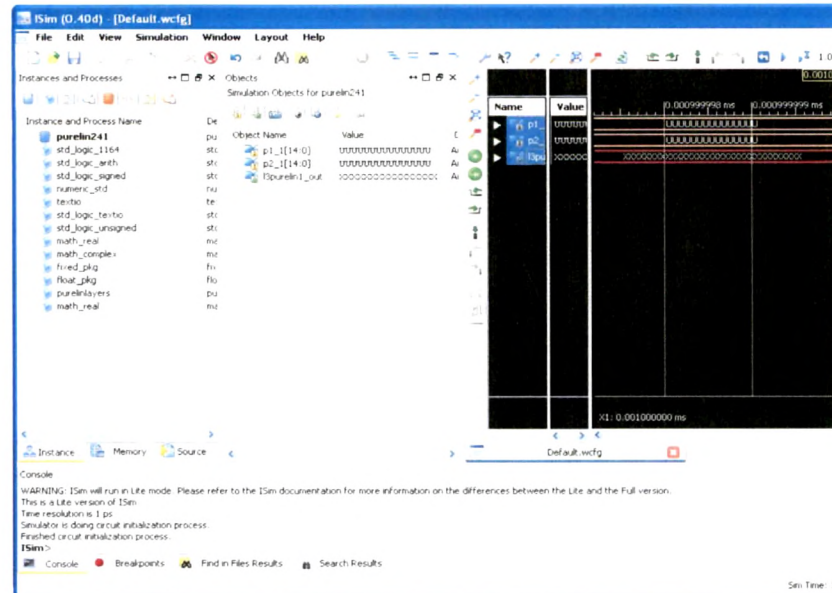


Figure A.7: ISim Graphical User Interface

## A.2 Impact Setup

The Digilent Plug-in for Xilinx tools allows Xilinx software tools to directly use the Digilent USB-JTAG FPGA configuration circuitry. For 14.x, Xilinx Impact, ChipScope Pro, EDK Xilinx Microprocessor Debugger (XMD) command line mode, and EDK Xilinx Software Development Kit (SDK) are currently supported by the Plug-in. Refer to <http://www.xilinx.com/> for more information about these Xilinx design tools.

### Software Versions Tested:

- ❖ Xilinx ISE Design Suite Version 14.x only (Refer to <http://www.digilentinc.com/> for versions of the plugin for later Xilinx ISE versions)
- ❖ Digilent Adept System 2.9 (or Digilent Adept Runtime 2.9 for Linux) or greater

Supported Operating Systems:

Microsoft Windows 32-bit and 64-bit Operating Systems  
Linux: Red Hat and CentOS 4, 5, 6 (x86/x64), and SUSE 11 (x86/x64)

### ⚡ Plug-In Installation

To begin, ensure that Xilinx ISE Suite (14.x only) and Digilent Adept System 2.9 (or greater) for Windows, or Digilent Adept Runtime 2.9 (or greater) for Linux, is

installed on the host computer. For Windows Systems also ensure that Microsoft Visual C++ 2008 Service Pack 1 Redistributable Package MFC Security Update is installed on the host computer. The Visual C++ Package is available for download at the following website: <http://www.microsoft.com/en-us/download/details.aspx?id=26368>

The plug-in files **libCseDigilent.dll** and **libCseDigilent.xml** must be copied to a location that is searched by the ISE Suite. Xilinx Impact is used to download bitstreams to FPGA boards. The following steps show how to use Impact with the Plug-in.

- 1. Launch Impact, double click on “Boundary Scan”, and select the “Cable Setup...” menu item from the “Output” menu.(Refer Figure A.8)

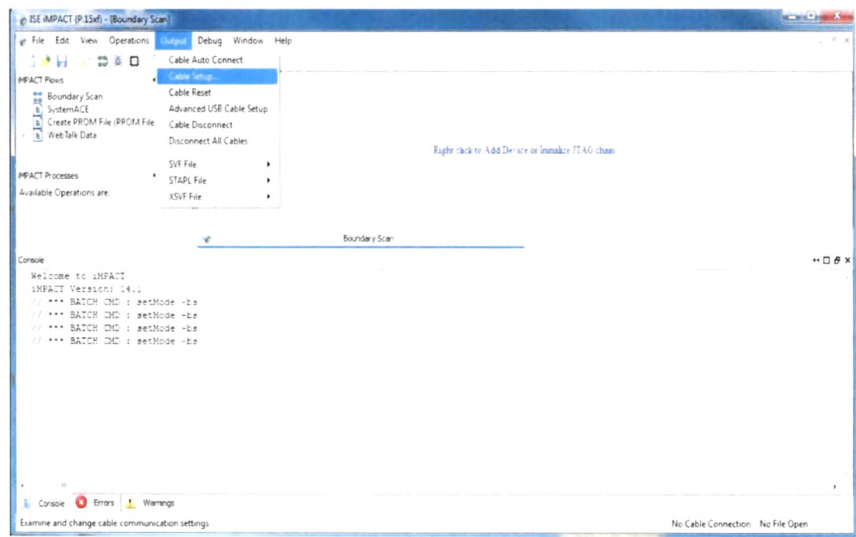


Figure A.8: Cable Set up

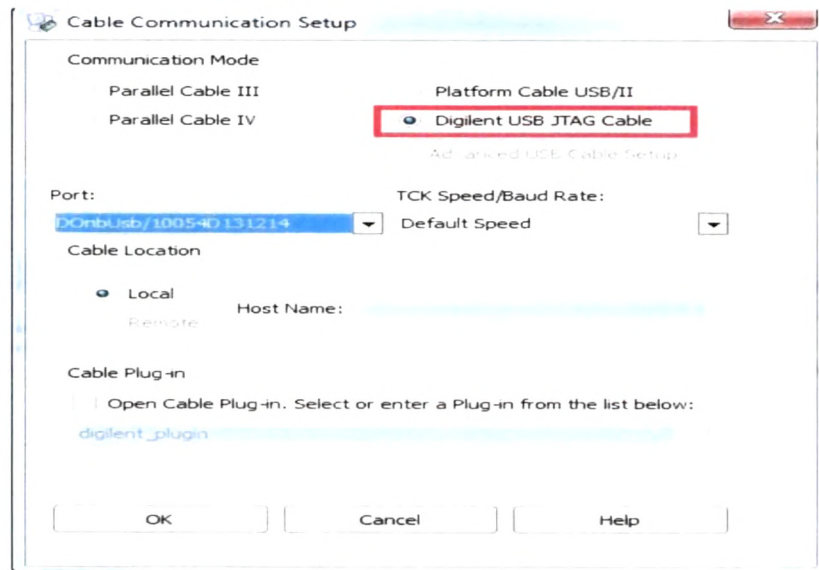
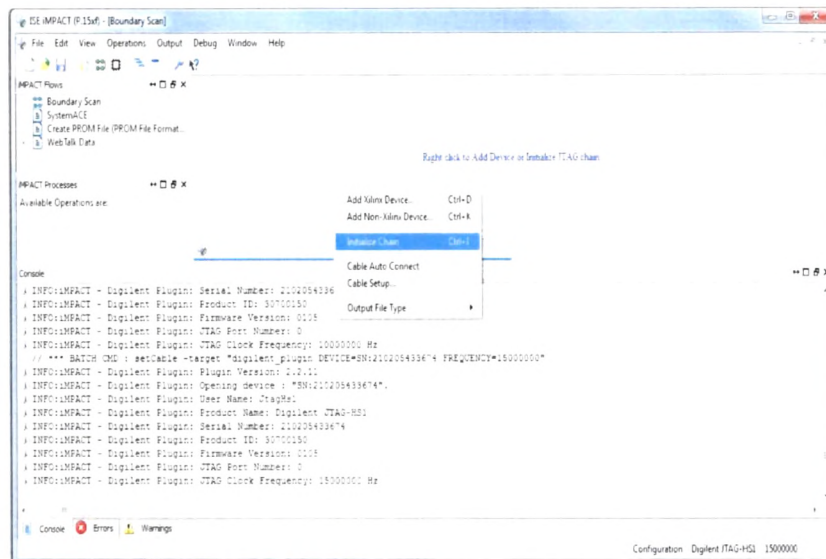


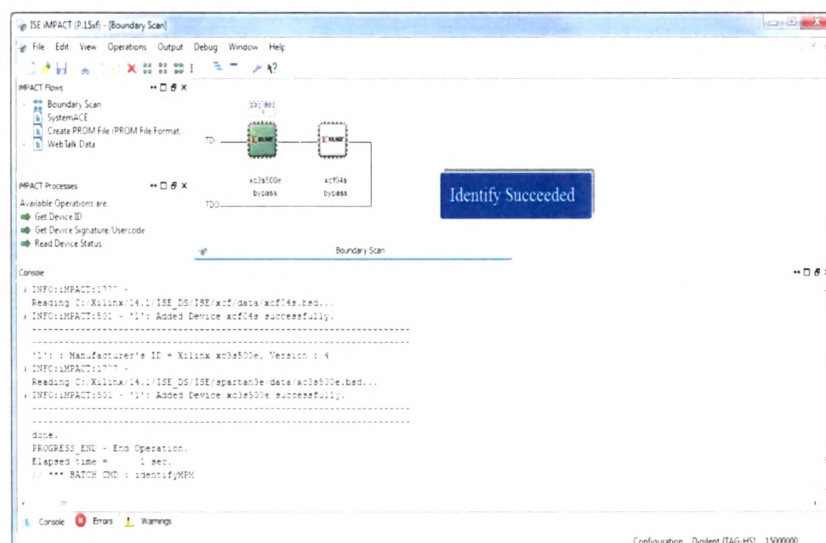
Figure A.9: Cable Communication Setup

2. Select “Digilent USB JTAG Cable” for the “Communication Mode” as shown in Figure A.9.
3. The “Port:” drop-down list should now contain a list of available devices. Select a device to connect to. Click on “OK” and proceed.
4. Right Click in the “Boundary Scan” window to and then click on “Initialize Chain”. (Refer Figure A.10)



**Figure A.10: Snapshot of Boundary Scan**

5. Impact is now ready to communicate with the FPGA on the board. Now double click on program option by right click on target device or double click on program in “**Impact Processes**” Pane, Which will now program the FPGA Chip and display the message as shown in Figure A.11.



**Figure A.11: Program Launch Window**

### A.3 Atlys™ Board: Spartan-6 XC6SLX45 CSG324C

The Spartan-6 LX45 is optimized for high-performance logic and offers:

- ✧ 6,822 slices, each containing four 6- input LUTs and eight flip-flops
- ✧ 2.1Mbits of fast block RAM
- ✧ four clock tiles (eight DCMs & four PLLs)
- ✧ six phase-locked loops
- ✧ 58 DSP slices
- ✧ 500MHz+ clock speeds

#### Features:

- ✧ Xilinx Spartan-6 LX45 FPGA, 324-pin BGA package
- ✧ 128Mbyte DDR2 with 16-bit wide data
- ✧ 10/100/1000 Ethernet PHY
- ✧ on-board USB2 ports for programming and data transfer
- ✧ USB-UART and USB-HID port (for mouse/keyboard)
- ✧ two HDMI video input ports and two HDMI output ports
- ✧ AC-97 Codec with line-in, line-out, mic, and headphone
- ✧ real-time power monitors on all power rails
- ✧ 16Mbyte x4 SPI Flash for configuration and data storage
- ✧ 100MHz CMOS oscillator
- ✧ 48 I/O's routed to expansion connectors
- ✧ GPIO includes eight LEDs, six buttons, and eight slide switches
- ✧ ships with a 20W power supply and USB cable

### A.4 Programming WSN Notes

#### 1. Programmer's Notepad 2

MoteWorks includes a version of Programmer's Notepad (PN2) that is configured as a simple IDE for nesC code.

- ✧ Steps for implementing WSN application on PN2
1. Open Programmer's Notepad from Start>Programs>Crossbow>PN
  2. Open a nesC file within an application directory. (eg. MyApp.nc), and click on Tools > make MICAz. It can also be executed in the shell commands by clicking on Tools > shell and then typing the command in the dialog box. The "Output" section of the Programmers Notepad will print the compiling results to the screen as shown in Figure A.12.



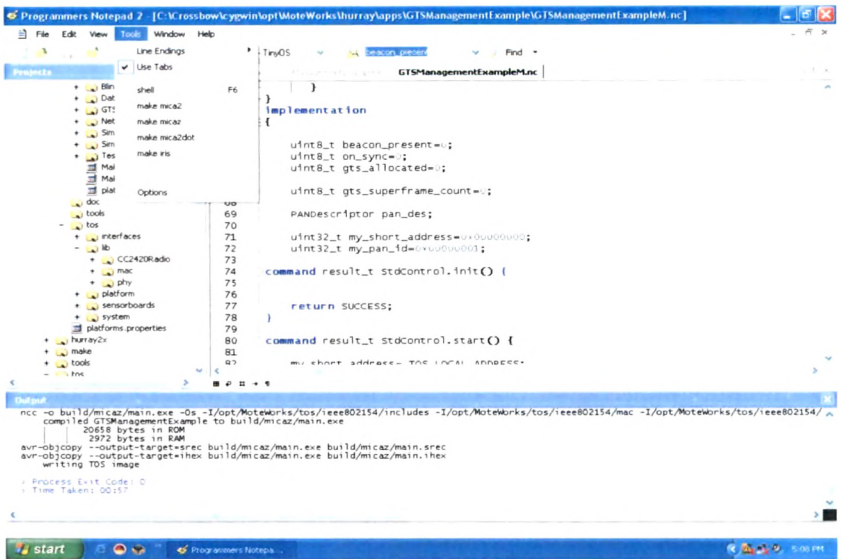


Figure A.12: Snapshot of Programming Notepad 2

After the compilation has completed one should see “writing TOS image” as the last line in the Output window. If we don’t see this then we have made an error typing in one of our files.

- 3. Application can be installed to a Mote plugged into programming board using Programmer’s Notepad. To install application:

Select Tools > shell. When prompted for parameters, type in **make micaz reinstalls mib520, com10**. The “Output” section of the Programmers Notepad will print the installation results to the screen as shown in Figure A.13.

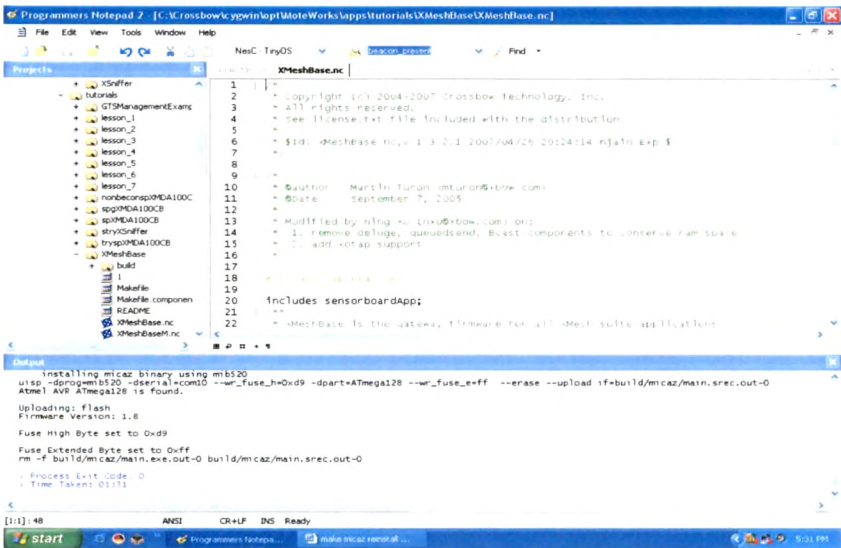


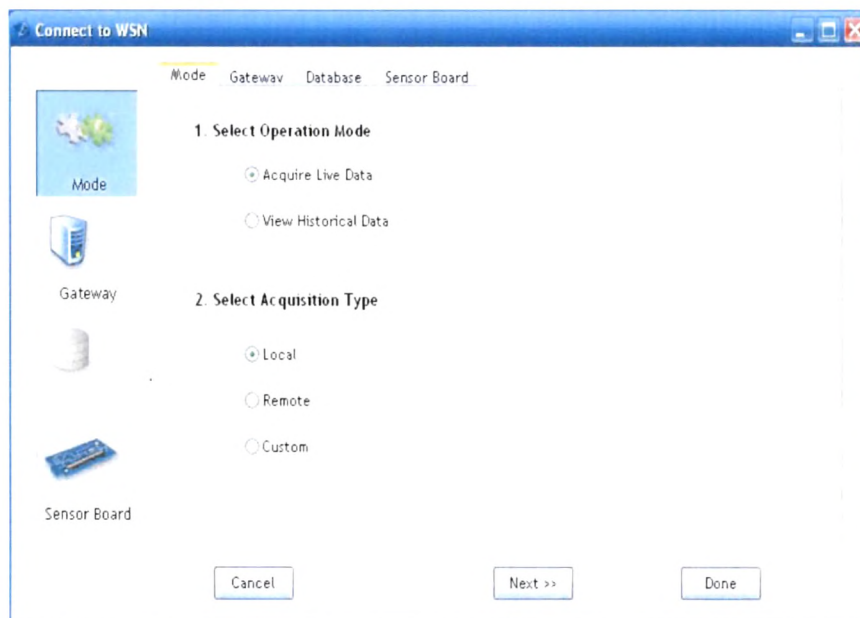
Figure A.13: Output Section of PN2

MoteWorks includes tool named MoteView that can be used to eavesdrop on messages sent over the Mote radios.

## 2. MOTE-VIEW

MoteView is designed to be an interface between a user and a deployed network of wireless sensors. MoteView provides the tools to simplify deployment and monitoring. It also makes it easy to connect to a database, to analyse, and to graph sensor readings. The key function of the program is to monitor the communications between the gateway and the individual motes. The data can be displayed using the MoteView program.

1. Start MoteView to configure the settings.
2. Start MoteView software, click on “Connect to WSN” icon in the upper left of the panel. The following Figure A.14 is the pop-up window, in the Mode tab, select acquire live data as operation mode.



**Figure A.14: Mode Configurations**

3. In the Gateway tab (Figure A.15), select MIB520 from interface board, COM10 as serial port, and select 57600 as baud rate.

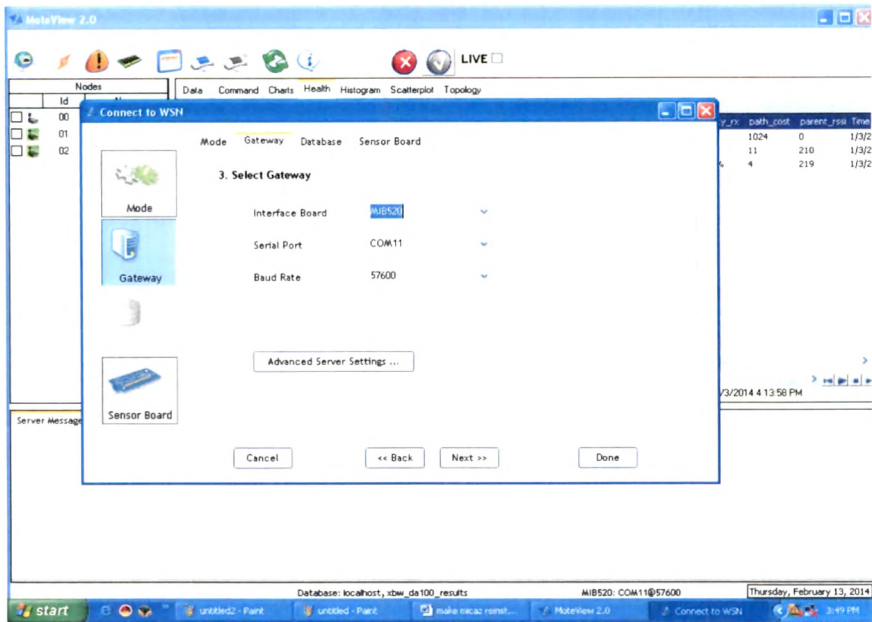


Figure A.15: Gateway Configuration

4. In the Database tab (Figure A.16), localhost is the database server; database name task was created during the PostgreSQL installation.

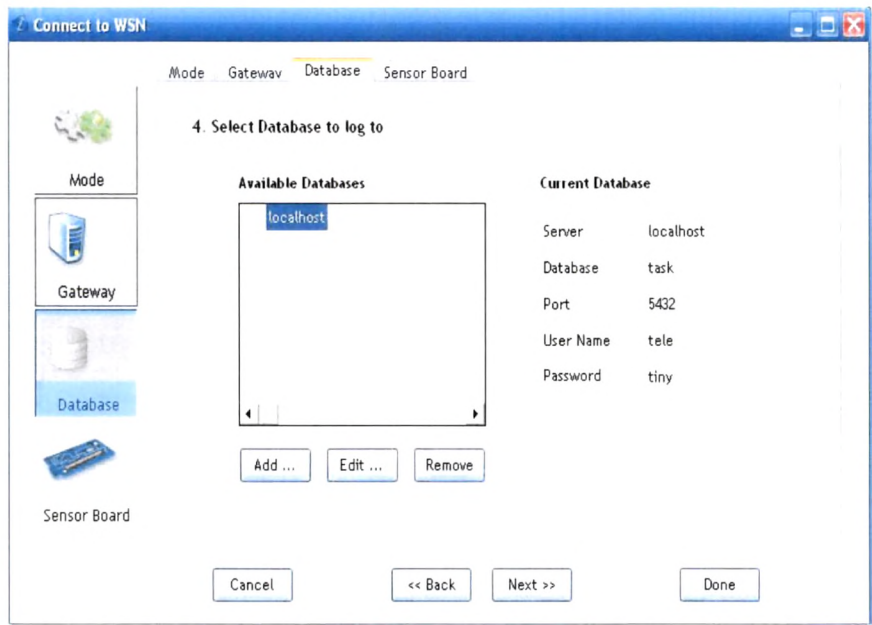
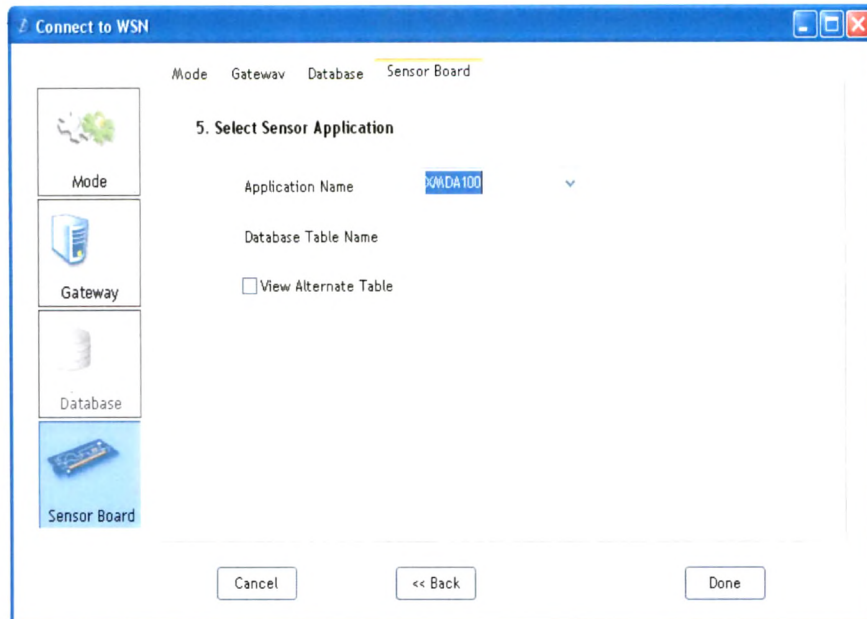


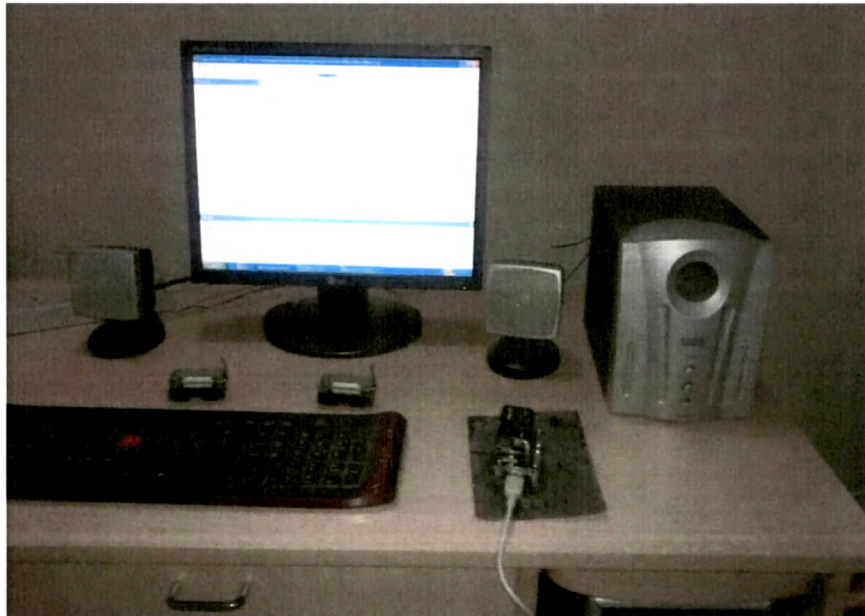
Figure A.16: Database Configurations

5. In the Sensor Board tab (Figure A.17), select XMDA100 from the application name drop list. Then, click “Done”. MICAz nodes are flashing and MIB520 base station start to collect data from sensor nodes.



**Figure A.17: Sensor Board Configurations**

The complete set up for WSN application is shown in following Figure A.18



**Figure A.18: MICAz Nodes & Gateway Setup**