ANNEXURE-I

DATASHET OF TMS320F2806 DSP

1 Features

- High-Performance Static CMOS Technology
  - 150 MHz (6.67-ns Cycle Time)
  - Low-Power (1.8-V Core @135 MHz, 1.9-V Core @150 MHz, 3.3-V I/O) Design
- JTAG Boundary Scan Support†
- High-Performance 32-Bit CPU (TMS320C28x)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Atomic Operations
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - 4M Linear Program/Data Address Reach
  - Code-Efficient (in C/C++ and Assembly)
  - TMS320F24x/LF240x Processor Source Code Compatible
- On-Chip Memory
  - Flash Devices: Up to 128K x 16 Flash (Four 8K x 16 and Six 16K x 16 Sectors)
  - ROM Devices: Up to 128K x 16 ROM
  - 1K x 16 OTP ROM
  - L0 and L1: 2 Blocks of 4K x 16 Each Single-Access RAM (SARAM)
  - H0: 1 Block of 8K x 16 SARAM
  - M0 and M1: 2 Blocks of 1K x 16 Each SARAM
- Boot ROM (4K x 16)
  - With Software Boot Modes
  - Standard Math Tables
- External Interface (2812)
  - Up to 1M Total Memory
  - Programmable Wait States
  - Programmable Read/Write Strobe Timing
  - Three Individual Chip Selects
- Clock and System Control
  - Dynamic PLL Ratio Changes Supported
  - On-Chip Oscillator
  - Watchdog Timer Module
- Three External Interrupts
- Peripheral Interrupt Expansion (PIE) Block That Supports 45 Peripheral Interrupts
- Three 32-Bit CPU-Timers
- 128-Bit Security Key/Lock
  - Protects Flash/ROM/OTP and L0/L1 SARAM
  - Prevents Firmware Reverse Engineering
- Motor Control Peripherals
  - Two Event Managers (EVA, EVB)
  - Compatible to 240xA Devices
- Serial Port Peripherals
  - Serial Peripheral Interface (SPI)
  - Two Serial Communications Interfaces (SCIs), Standard UART
  - Enhanced Controller Area Network (eCAN)
  - Multichannel Buffered Serial Port (McBSP)
- 12-Bit ADC, 16 Channels
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Fast Conversion Rate: 80 ns/12.5 MSPS
- Up to 56 General Purpose I/O (GPIO) Pins
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Development Tools Include
  - ANSI C/C++ Compiler/Assembler/Linker
  - Code Composer Studio™ IDE
  - DSP/BIOS™
  - JTAG Scan Controllers†
- Low-Power Modes and Power Savings
  - IDLE, STANDBY, HALT Modes Supported
  - Disable Individual Peripheral Clocks
- Package Options
  - 179-Ball MicroStar BGA™ With External Memory Interface (GHH), (ZHH) (2812)
  - 176-Pin Low-Profile Quad Flatpack (LQFP) With External Memory Interface (PGF) (2812)
  - 128-Pin LQFP Without External Memory Interface (PBK) (2810, 2811)
- Temperature Options:
  - A: –40°C to 85°C (GHH, ZHH, PGF, PBK)
  - S/Q: –40°C to 125°C (GHH, ZHH, PGF, PBK)

TMS320C24x, Code Composer Studio, DSP/BIOS, and MicroStar BGA are trademarks of Texas Instruments.
† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port

Table 2-1. Hardware Features (100-MHz Devices)

FEATURE		F2809	F2808	F2806	F2802	F2801/ 9501	C2802	C2801
Instruction cycle (at 100 MHz)		10 ns	10 ns	10 ns	10 ns	10 ns	10 ns	10 ns
Single-access RAM (SARAM) (16-bit word)		18K (L0, L1, M0, M1, H0)	18K (L0, L1, M0, M1, H0)	10K (L0, L1, M0, M1)	6K (L0, M0, M1)	6K (L0, M0, M1)	6K (L0, M0, M1)	6K (L0, M0, M1)
3.3-V on-chip flash (16-bit word)		128K	64K	32K	32K	16K	–	–
On-chip ROM (16-bit word)		–	–	–	–	–	32K	16K
Code security for on-chip flash/SARAM/OTP blocks		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Boot ROM (4K X16)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
One-time programmable (OTP) ROM (16-bit word)		1K	1K	1K	1K	1K	–	–
PWM outputs		ePWM1/2/3/4/5/6	ePWM1/2/3/4/5/6	ePWM1/2/3/4/5/6	ePWM1/2/3	ePWM1/2/3	ePWM1/2/3	ePWM1/2/3
HRPWM channels		ePWM1A/2A/3A/ 4A/5A/6A	ePWM1A/2A/ 3A/4A	ePWM1A/2A/ 3A/4A	ePWM1A/2A/3A	ePWM1A/2A/3A	ePWM1A/2A/3A	ePWM1A/2A/3A
32-bit CAPTURE inputs or auxiliary PWM outputs		eCAP1/2/3/4	eCAP1/2/3/4	eCAP1/2/3/4	eCAP1/2	eCAP1/2	eCAP1/2	eCAP1/2
32-bit QEP channels (four inputs/channel)		eQEP1/2	eQEP1/2	eQEP1/2	eQEP1	eQEP1	eQEP1	eQEP1
Watchdog timer		Yes	Yes	Yes	Yes	Yes	Yes	Yes
12-Bit, 16-channel ADC conversion time		80 ns	160 ns	160 ns	160 ns	160 ns	160 ns	160 ns
32-Bit CPU timers		3	3	3	3	3	3	3
Serial Peripheral Interface (SPI)		SPI-A/B/C/D	SPI-A/B/C/D	SPI-A/B/C/D	SPI-A/B	SPI-A/B	SPI-A/B	SPI-A/B
Serial Communications Interface (SCI)		SCI-A/B	SCI-A/B	SCI-A/B	SCI-A	SCI-A	SCI-A	SCI-A
Enhanced Controller Area Network (eCAN)		eCAN-A/B	eCAN-A/B	eCAN-A	eCAN-A	eCAN-A	eCAN-A	eCAN-A
Inter-Integrated Circuit (I^2C)		I^2C-A	I^2C-A	I^2C-A	I^2C-A	I^2C-A	I^2C-A	I^2C-A
Digital I/O pins (shared)		35	35	35	35	35	35	35
External interrupts		3	3	3	3	3	3	3
Supply voltage	1.8-V Core, 3.3-V I/O	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Packaging	100-Pin PZ	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	100-Ball GGM, ZGM	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Temperature options(1)	A: -40°C to 85°C	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)
	S: -40°C to 125°C	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)	(PZ, GGM, ZGM)
	Q: -40°C to 125°C	(PZ)	(PZ)	(PZ)	(PZ)	(PZ)	(PZ)	(PZ)
Product status(2)		*TMX*	TMS	TMS	TMS	TMS	TMS	TMS

(1) The UCD9501 device is not available in the Q temperature option or in ZGM/GGM packages.
(2) See Section 5.1, Device and Development Support Nomenclature for descriptions of device stages. TMX is an experimental device that is not necessarily representative of the final device's electrical specifications. TMS is a fully qualified production device. For UCD9501, the production qualified device is labeled UCD9501.