CHAPTER-3
GRID SYNCHRONIZATION FOR THREE-PHASE GRID-TIED CONVERTER

The power grid is a complex dynamic system that is affected by a variety of events, such as continuous variation in the connection of electrical loads, interference and resonance due to harmonic currents flowing through the line, faults caused by lightning strikes, and errors in the operation of electrical equipment. Therefore, when the power converter is connected to the power grid, the grid variable cannot be regarded as a constant amplitude and constant frequency, but it should be continuously monitored to ensure the desired performance of the grid connected power converter. The basic amplitude, frequency, and phase-angle information become the key controllable parameters for the effective operation of the grid-connected converter (GCC) [67]. For this reason, the control algorithm based on the concept of grid synchronization is very important for estimating the grid voltage parameters required for GCC control, protection and synchronization. The phase-angle of the grid voltage is critical and essential parameter for the control system of grid-connected power converters, because popular control strategies (for example, direct power control, vector oriented control) strongly depend on the phase angle of the grid voltage to achieve Park transformation (dq reference frame conversion). The synchronous frame voltages (voltages at dq reference frame) are key parameter for the control system to decouple the current control loop under the dq reference frame[68]. Therefore, the grid synchronization technology is a basic component of the grid-connected converter control strategy, and it is very important to ensure the satisfactory performance of the converter. In order to achieve precise and fast synchronization, many different grid synchronization technologies have been intensively studied and proposed [67-69]. It should be noted that the grid voltage during grid synchronization may be under normal or abnormal conditions (i.e. 1-Φ phase grid voltage, 3-Φ phase unbalanced grid voltage, 3-Φ phase distortion grid voltage, phase-angle jump, frequency shift), and in the above method, PLL and FLL are crucial techniques to compute the utility grid parameters. However, interrelated feedback can be observed in these technologies, which may affect the tuning process

as well as the stability margin and of the entire control scheme [8][70]. The conventional three-phase PLL, commonly known as synchronous reference frame (SRF), has excellent performance during the ideal grid situation (i.e. balanced grid voltage). However, if the measured grid voltage signal is unbalanced or distorted, it will give oscillatory response of computed fundamental frequency [70-72]. The decouple synchronous reference frame PLL (DDSRF-PLL) technique reported in the literature [8] improves the poor performance of the traditional SRF based PLL. The DDSRF-PLL extracts positive and negative sequence components from the non-ideal grid voltages to compute the frequency. However, the performance of DDSRF-PLL will decrease during the highly distorted grid voltages. It can be found that under this distorted grid signal condition, the phase detector (PD) structure based on the generalized integrator (GI) has better performance and reliability [8][74-75]. Thus, the second-order generalized integrator based PLL (SOGI-PLL) is superior over the above-described PLLs and gives fast and accurate frequency and phase-angle estimation under the adverse grid conditions. Instead of the estimated frequency signal from the SOGI-PLL feed-backed to the SOGI block structure, this frequency can be computed adaptively by the frequency-locked loop (FLL) structure, added in SOGI structure and combination is known as SOGI-FLL, to obtain excellent performance over the SOGI-PLL[76]. Instead of PLL, tan-arc phase-angle computation is used to compute the phase-angle and the adaptive feature of FLL improves performance [77]. Two SOGI blocks connected in parallel form a dual SOGI-FLL (DSOGI-FLL) structure, which can provide good transient response even in the presence of grid abnormalities (harmonics distortions, voltage imbalances, frequency changes, voltage imbalances). The performance of the DSOGI-FLL is analyzed in the presence of different grid voltage abnormalities. The DSOGI-FLL is not able to extract precise phase-angle in presence of DC-offset

3.1 Phase Lock Loop

Figure 3-1 depicts the components of a digitally implemented PLL, as shown in the block diagram: Relying on the PI controller and linear integration, the Loop Filter acts as a low-pass filter, while the Phase Detector is accomplished by means of the multiplier.

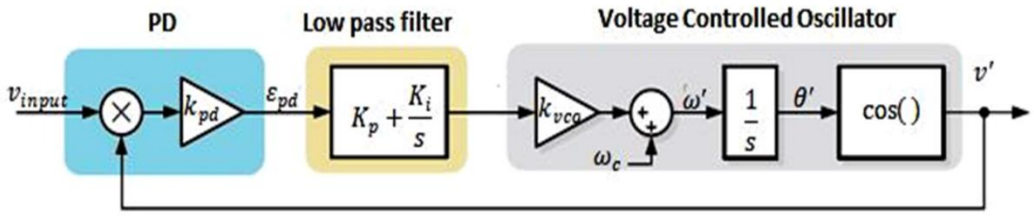


Figure 3- 1 : Phase lock loop block diagram[8]

The output of Phase detector is given as:

$$v_{pd} = V_{peak} \sin\theta * \cos\theta' = V_{peak} \sin(\omega t + \emptyset) * \cos(\omega' t + \emptyset') = \frac{V_{peak}}{2}[\sin((\omega - \omega')t + (\emptyset - \emptyset')) + \sin((\omega + \omega')t + (\emptyset + \emptyset'))] \quad (3.1)$$

The phase error signal ε_{PD} can be expressed as follows:

$$\varepsilon_{PD} = \frac{V_{peak}}{2} K_{pd} \left[\underbrace{\sin((\omega - \omega')t + (\emptyset - \emptyset'))}_{\text{Low-frequency term}} + \underbrace{\sin((\omega + \omega')t + (\emptyset + \emptyset'))}_{\text{high-frequency term}}\right] \quad (3.2)$$

Due to the low-pass filter and VCO being tuned to input frequency i.e.,$\omega \approx \omega'$, the DC component of ε_{PD} signals is presented as an example.

$$\widetilde{\varepsilon_{PD}} = \frac{V_{peak}}{2} K_{pd} \sin(\emptyset - \emptyset') \quad (3.3)$$

Non-linear phase detection is the result of the sinusoidal function in equation (3.3). For phase detection purposes, however, when the ε_{PD} is extremely tiny, the output of the multiplier PD becomes linear in this way: $\sin(\emptyset - \emptyset') \approx \sin(\theta - \theta') \approx (\theta - \theta')$, and is supplied as a linear function of the phase error, expressed as:

$$\widetilde{\varepsilon_{PD}} = \frac{V_{peak}}{2} K_{pd}(\theta - \theta') \quad (3.4)$$

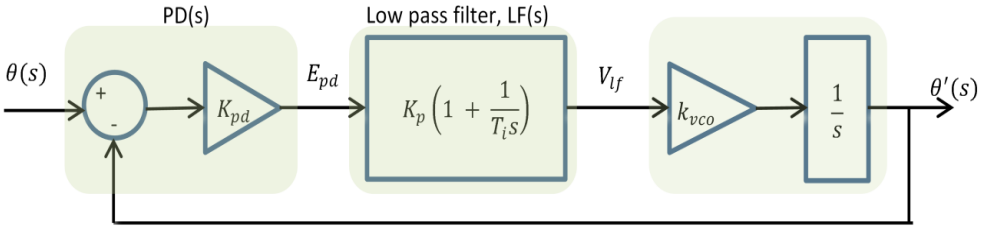


Figure 3- 2 Phase lock loop Linearized block diagram in the complex frequency domain

Figure 3-2 illustrates the Laplace transformation being used to transform the above equation from the continues–time domain to the complex frequency domain. For the second-order transfer functions for PLL from the Figure 3-2, the $H_\theta(s)$ the average frequency of VCO ($\widetilde{\omega}'$), and $E_\theta(s)$ are expressed as functions:

$$H_\theta(s) = \frac{\theta'(s)}{\theta(s)} = \frac{K_p s + \frac{K_p}{T_i}}{s^2 + K_p s + \frac{K_p}{T_i}} \quad ; \quad H_\theta(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.5}$$

$$E_\theta(s) = \frac{E_{pd}(s)}{\theta(s)} = \frac{s^2}{s^2 + K_p s + \frac{K_p}{T_i}} \quad ; \quad E_\theta(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.6}$$

$$\widetilde{\omega}' = (\omega_0 + \Delta\,\widetilde{\omega}') = (\omega_0 + k_{vco}\widetilde{v_{lf}}) \tag{3.7}$$

Where $\omega_0$is the centre frequency of the VCO as a feed-forward, $\omega_n = \sqrt{\frac{K_p}{T_i}}$, and $\zeta = \frac{\sqrt{K_p T_i}}{2}$.

Using the given frequency range, the signal's phase should be determined, as follows:

$$\tilde{\theta}'(t) = \int \widetilde{\omega}'\ dt = \int k_{vco}\widetilde{v_{lf}}\ dt \tag{3.8}$$

The output signal is sent back to the input side of the multiplier PD, which implies that the average output must be zero. It might be achieved by adjusting the center frequency to match the output signal's frequency. With two poles at origin, this form of system can track continual slope without having to deal with the steady-state error. The settling time of a second-order system may be estimated by the time it takes to settle within 1% of its steady state response for a given step input, and mathematically is describe as:

$$t_s = 4.6\,\tau \quad ; \quad \text{where } \tau = \frac{1}{\xi\omega_n} \tag{3.9}$$

Pull-in ranges $\Delta\omega_p$ merely the frequency at which a PLL will always be locked into a stable state. A pull-in process begins after an input frequency change, and the time it takes for the PLL to achieve a locked state may be expressed as:

$$t_p \approx \frac{\pi^2}{16}\frac{\Delta\omega_{in}^2}{\xi\omega_n^3} \tag{3.10}$$

The bandwidth of PLL can be express as:

$$\omega_{-3dB} = \omega_n[1 + 2\xi^2 + \sqrt{(1+2\xi)^2 + 1}]^{\frac{1}{2}} \tag{3.11}$$

As demonstrated in Figure 3-2, the PLL in Figure 3-3 performs well with single phase grids at 50Hz with settling time t_s=100ms and $\xi = 1/\sqrt{2}$. At t = 150 ms, the frequency shifts from 50Hz to 45Hz and the phase angle from 0^o to $+45^o$. The grid frequency is quite close to the PLL cut-off frequency.

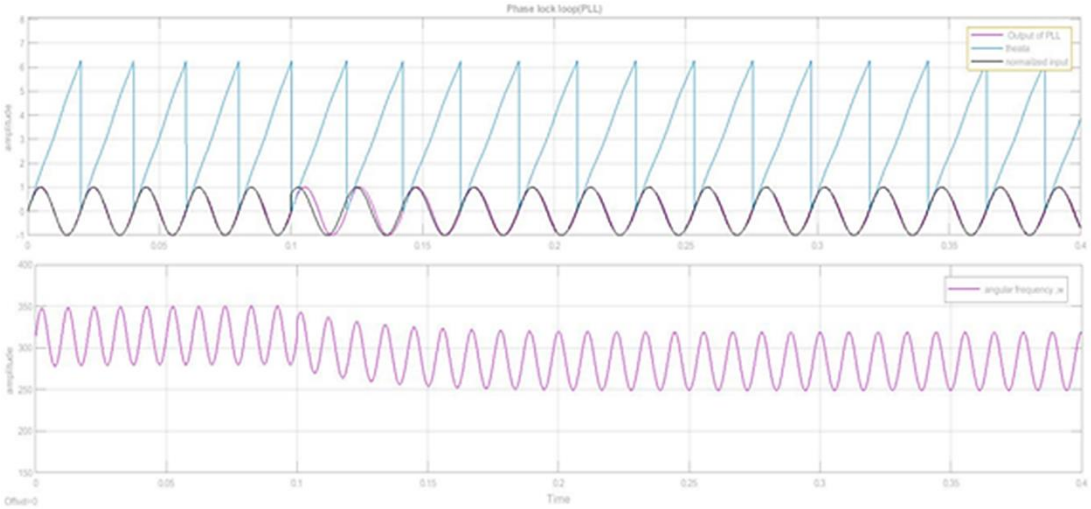


Figure 3- 3 Step response of Phase lock loop

One restriction is that $\omega_{in} - \omega_{vco}$ must be less than $\omega_p$and input signal frequency must be larger than the PLL bandwidth. Thus, higher frequency term of PD can be removed while examining PLL dominating dynamic response. As seen in equation (3.11), the PLL $\omega_{-3dB} = 21.3$ Hz has a bandwidth close to the grid frequency, which is 50Hz. PLL locking results in a high frequency term in the phase-angle error (ε_{PD}) of only twice the input frequency, which is 100Hz in this case For a single-phase grid-tied system, a PLL design based on an in-quadrature signal should be utilized in order to eliminate the 100Hz oscillation in the phase-angle error signal.

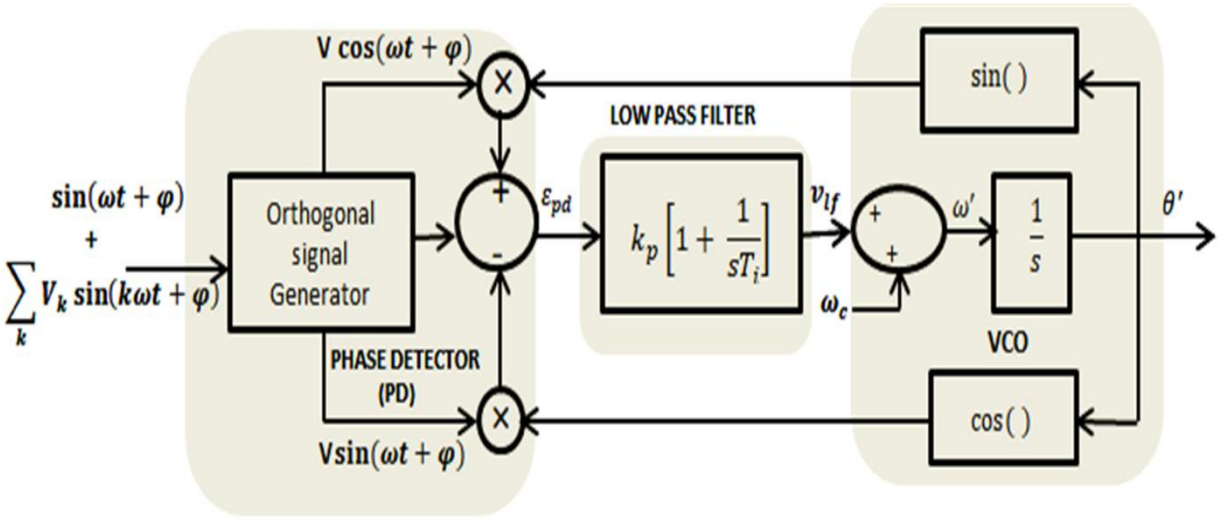


Figure 3- 4 Block diagram of PLL with quadrature signal generator and two phase detector

The in-quadrature phase detector of the PLL yields the phase-angle error signal ε_{PD}, which is given by

$$\varepsilon_{PD} = V\{\sin(\omega t + \emptyset) * \cos(\omega' t + \emptyset') - \cos(\omega t + \emptyset) * \sin(\omega' t + \emptyset')\} = V\big((\omega - \omega')t + (\emptyset - \emptyset')\big) = V\sin(\theta - \theta') \quad (3.12)$$

A steady-state oscillatory term is not generated when the PLL is well-synchronized, as shown in equation (3.12). This implies that the PLL bandwidth may be increased and the aforesaid anomalies in the computation of PLL key parameters can be eliminated.

3.1.1 Synchronous Reference Frame based Phase Look Loop (SRF-PLL)

To implement a PLL for a three-phase system, there are typically two approaches to use it. The first approach is to utilize three single phase PLLs for each phase to extract the phase angles. This structure does not necessitate the conversion from 3-phase abc space to dq space.

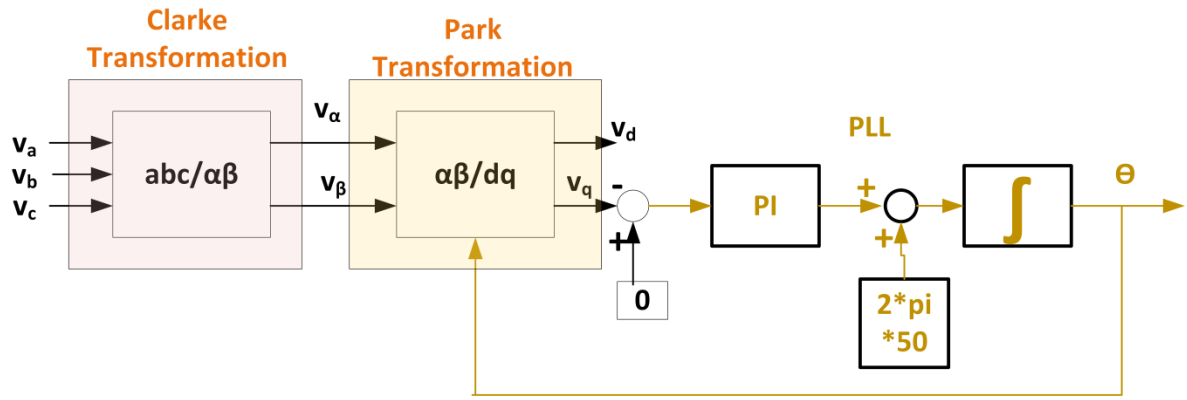


Figure 3- 5 Block diagram of SRF- PLL

The Clarke transformation (abc/αβ) transforms the three-phase grid voltages v_{abc} into the stationary frame's two-phase voltage$v_{\alpha\beta}$.

The accompanying voltage vector can be used to represent the transformation:

$$v_{(\alpha\beta)} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V\begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \quad (3.13)$$

$$v_{(dq)} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin\theta' & \cos\theta' \\ \cos\theta' & -\sin\theta' \end{bmatrix}\begin{bmatrix} V\sin\theta \\ V\cos\theta \end{bmatrix} \quad (3.14)$$

$$v_d = V\sin\theta\sin\theta' + V\cos\theta\cos\theta' = V\cos(\theta - \theta') \quad (3.15)$$

$$v_q = V \sin\theta \cos\theta' - V \sin\theta \sin\theta' = V\sin(\theta - \theta') \quad (3.16)$$

(a)

(b)

(c)

(d)

(e)

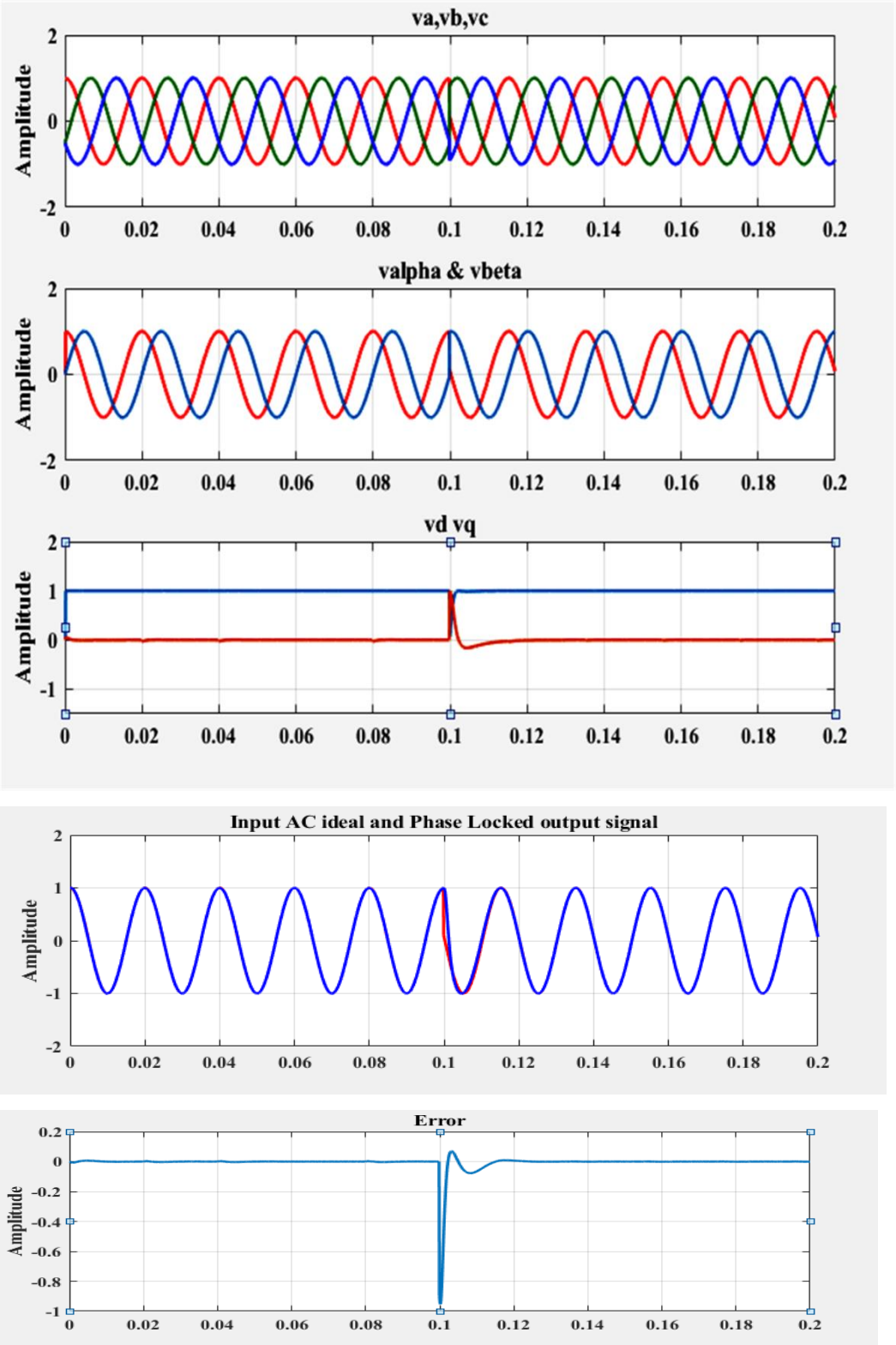


Figure 3- 6 Simulation results of SRF-PLL during Phase Jump of 90° at t=0.1 second

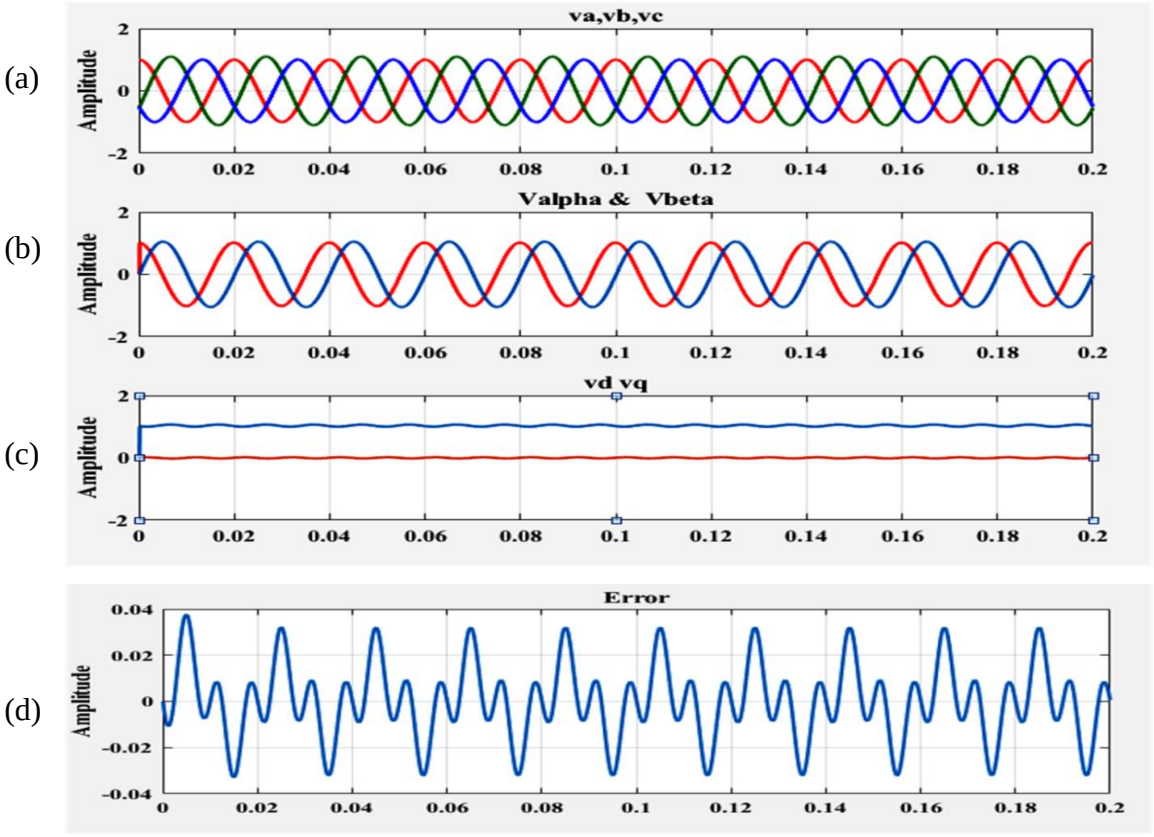


Figure 3- 7 Simulation results of SRF-PLL during voltage Imbalance of 10% on phase-B

The PI controller is used as a low-pass filter in the system. The low-pass filter accepts the q-axis component of grid voltage as an input (similarly as quadrature PLL in Figure 3-4), whereas the PI controller outputs the grid voltage angular speed. In order to accomplish dq axis decoupling, the PI controller adjusts the q-axis component of the grid voltage to zero, thus the grid voltage may be aligned with the d-axis and the q-axis component of the grid voltage is eliminated. An integrator is then used to acquire the phase angle of the grid voltage. A high bandwidth for the SRF-PLL feedback mechanism is necessary to quickly and precisely detect the phase angle and amplitude of the grid voltage under ideal grid conditions(i.e. balanced grid voltages for three phase system), that is, when unbalances and harmonic distortion have no effect on the grid voltage. Figure 3-6 (a) shows 3-phase grid voltage in per unit (p.u.) measurement. Figure 3-6(b) shows alpha –beta voltage waveform in stationary frame in per unit (p.u.) measurement by applying Clark transformation. Figure 3-6 (c) shows direct- quadrature voltage waveform in synchronous reference frame in per unit (p.u.) measurement by applying Park transformation. Figure 3.6 (d) & (e) show the output voltage signal of PLL locked with input voltage signal and

error signal from phase detector. Figure 3-6 depicts the response of an SRF-PLL tuned with a high gain, i.e. a wide bandwidth, to a 90° phase jump at t=0.1 second. By setting v_q= 0, as shown in Figure 3-5, the SRF-PLL instantaneously recognizes the balanced input voltage vector's amplitude and phase angle, virtually.When the grid voltage encountered a 10% voltage imbalance on phase B, the response of an SRF-PLL is depicted in Figure 3-7. The control loop bandwidth of this SRF-PLL was sufficiently high to make $v_q \approx 0$(Figure 3-7(c)), which means that the SRF-PLL could track the evolution of the unbalanced voltage vector applied to its input in real time. In this case, the measured phase angle causes oscillations to occur at a frequency twice as high as the input.

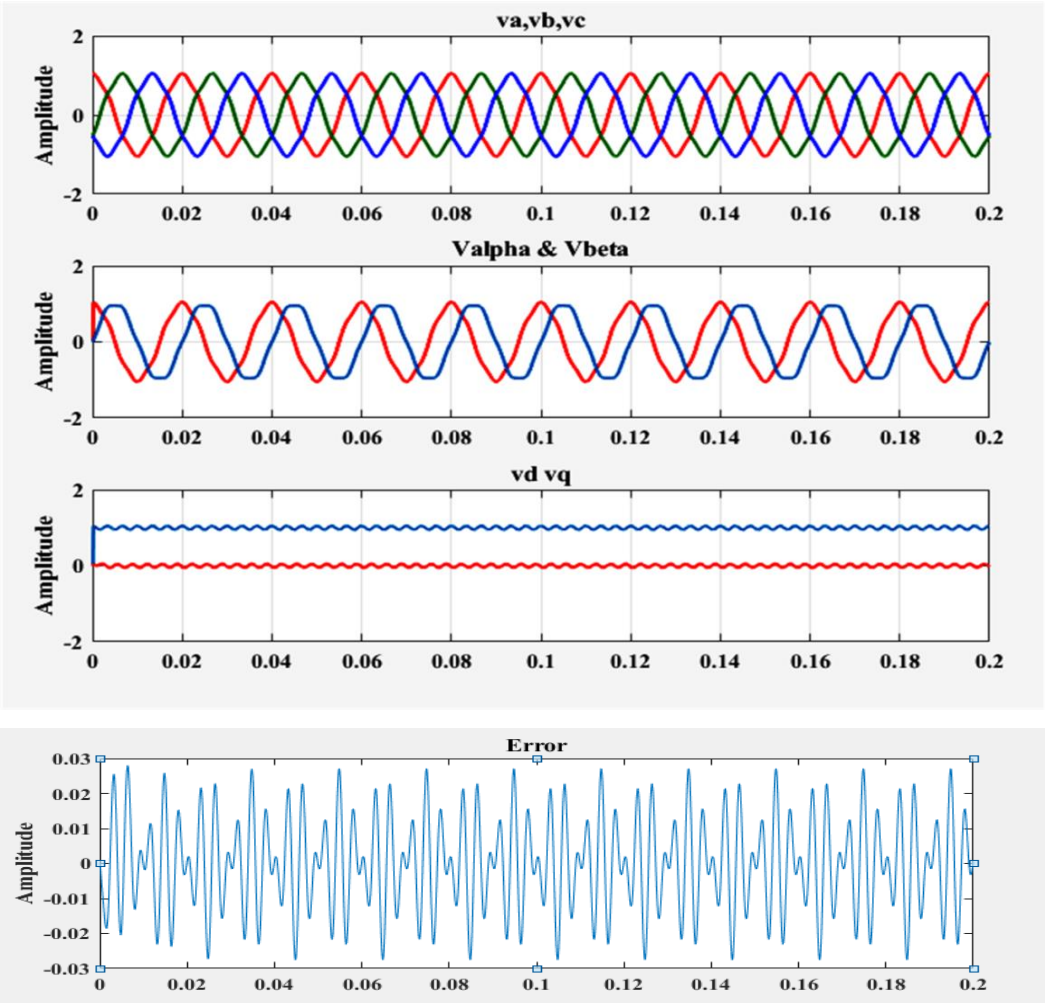


Figure 3-8: Simulation results of SRF-PLL during 5th Harmonic content in grid voltages (5%)

Figure 3-8 depicts the SRF-reaction PLL when a fifth-order harmonic is introduced to the three-phase voltage. As a result, $v_q \neq 0$ occurs when the SRF-PLL commits an

error (Figure 3-8(d)) while tracking the current position of the input voltage vector. Using pre-filtering in PLL or a method that matches the d-axis average voltage to the amplitude of the fundamental voltage in the positive-sequence, PLL automatically eliminate the fifth-order harmonic effect on dq angular position. As a result, a little reduction in the PLL bandwidth increases its performance, almost eliminating the influence of high-order harmonics on PLL output signals.

(a)

(b)

(c)

(d)

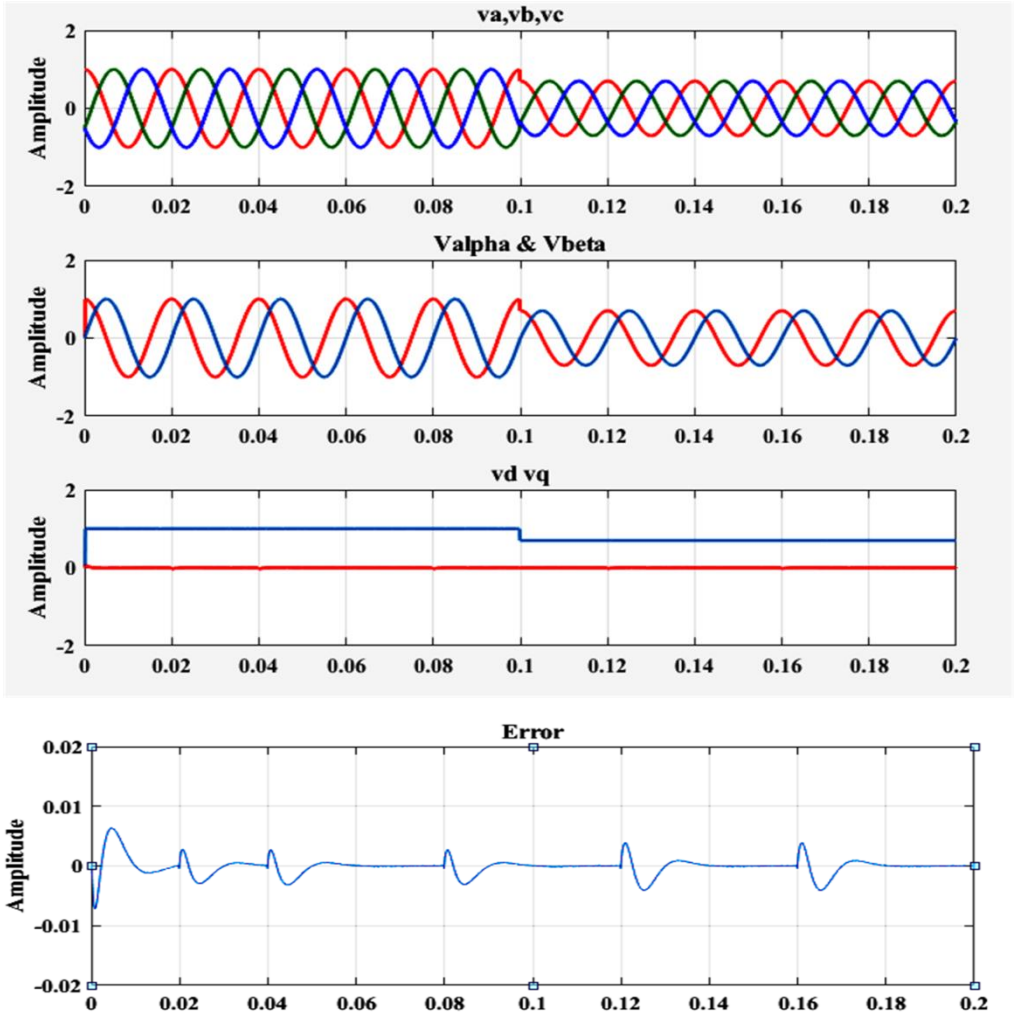


Figure 3- 9 Simulation results of SRF-PLL during balanced voltage change (Voltage Sags and Dips)

As shown in Figure 3-9, an SRF-PLL tuned for high gain, or wide bandwidth, responds to the presence of a three-phase balanced sag. As illustrated in Figure 3-9, the SRF-PLL immediately identifies the amplitude and phase angle of the balanced input voltage vector by setting $v_q = 0$ (Figure 3.9 (c)), virtually. It is not possible to

adequately analyze the positive-sequence component using typical filtering techniques to get the average value of v_d. SRF-PLL output signals may lead to a significant reduction in PLL bandwidth, as was previously discussed. A similar level of fifth harmonic distortion, as seen in Figure 3-8, affects the grid voltage. Figure 3-8(c) shows the oscillating error signal on both axes of the dq reference frame when the PLL is unable to instantaneously track the position of the fifth-order component. As a result, an average value of voltage on the d-axis (i.e. v_d) may be computed using a simple low-pass filter with a cut-off frequency of 20 Hz. When synchronizing with three-phase voltages polluted by high-order harmonics, reducing the PLL bandwidth is an effective method to obtain high-quality signals at the SRF-PLL output. It is not viable to adequately analyze the positive-sequence component using traditional filtering methods to get the average value of v_d.When synchronizing with three-phase voltages polluted by high-order harmonics, reducing the PLL bandwidth is an effective approach to generate high-quality signals at the SRF-PLL output, as shown in Figure 3-6, Figure 3-7, Figure 3-8, and Figure 3-9. However, the wind generating power station and PV power station use positive-sequence current injection at the fundamental frequency and eliminating injection of negative-sequence and harmonic currents for avoiding power fluctuations which cause damage in the power converter or inserts unbalanced reactive currents for grid compensation at a point of common coupling. A grid-connected three-phase power converter's major responsibility is to correctly detect the positive sequence component at the fundamental frequency of three-phase grid voltage.

3.2 Decouple Double Synchronous Reference Frame PLL (DDSRFPLL)

On the basis of rotation at both positive and negative synchronous frequencies, this section proposes an enhanced three-phase synchronized PLL. Even under unbalanced grid fault conditions, accurate grid synchronization can be achieved by using a double-synchronous reference frame, which decouples negative-sequence voltage components from positive-sequence voltage components. Variations in the grid circumstances cause phase voltage imbalances. Unbalanced three phase systems can be reduced to two symmetrical systems with zero components: one revolving in the

positive direction called the positive sequence and the other reversing it, or in the opposite direction called negative sequence (Figure 3-10). Park and Clarke transform imbalanced voltages are examined in the following section.

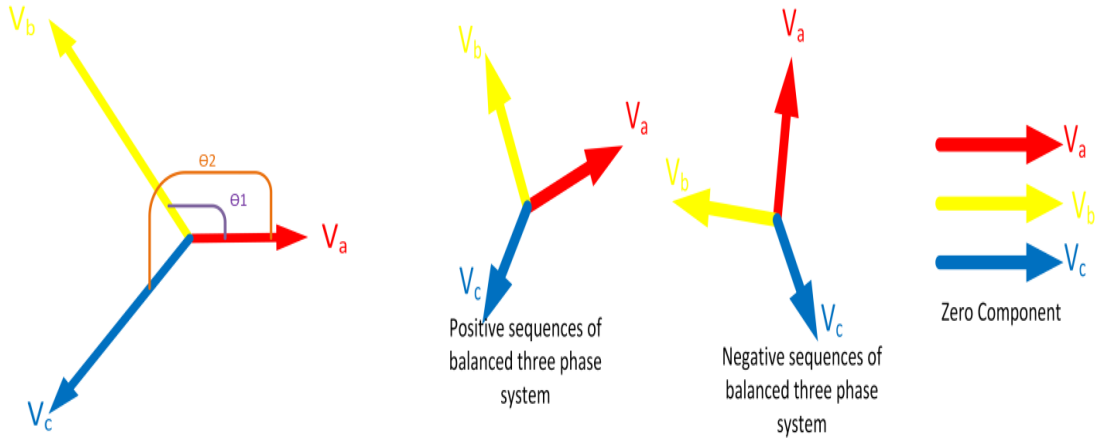


Figure 3- 10: Voltage vectors of unbalanced three phase system

$$v = v_{abc}^{+1} + v_{abc}^{-1} + v_{abc}^{0} \tag{3.17}$$

$$v = V_{+1}\begin{bmatrix}\cos(\omega t)\\ \cos(\omega t - \frac{2\pi}{3})\\ \cos(\omega t - \frac{4\pi}{3})\end{bmatrix} + V_{-1}\begin{bmatrix}\cos(\omega t)\\ \cos(\omega t - \frac{2\pi}{3})\\ \cos(\omega t - \frac{4\pi}{3})\end{bmatrix} + V_0\begin{bmatrix}1\\1\\1\end{bmatrix} \tag{3.18}$$

The voltage vector on a stationary reference frame can be expressed using the Clark transformation with respect to the positive sequences:

$$v_{\alpha\beta} = V_{+1}\begin{bmatrix}\cos(\omega t)\\ \sin(\omega t)\end{bmatrix} + V_{-1}\begin{bmatrix}\cos(-\omega t)\\ \sin(-\omega t)\end{bmatrix} \tag{3.19}$$

3.2.1 Double Synchronous Reference Frame

The unbalanced voltage vector's positive and negative sequence components are shown in Figure 3-11 , along with a double synchronous reference frame (DSRF) composed of two rotating reference frames: dq_{+1}, rotating at a positive angular frequency($+\omega$) and with an angular position of $+\theta_1$, and dq_{-1}, rotating at a

negative angular frequency($-\omega$) and with an angular position of $-\theta_1$.

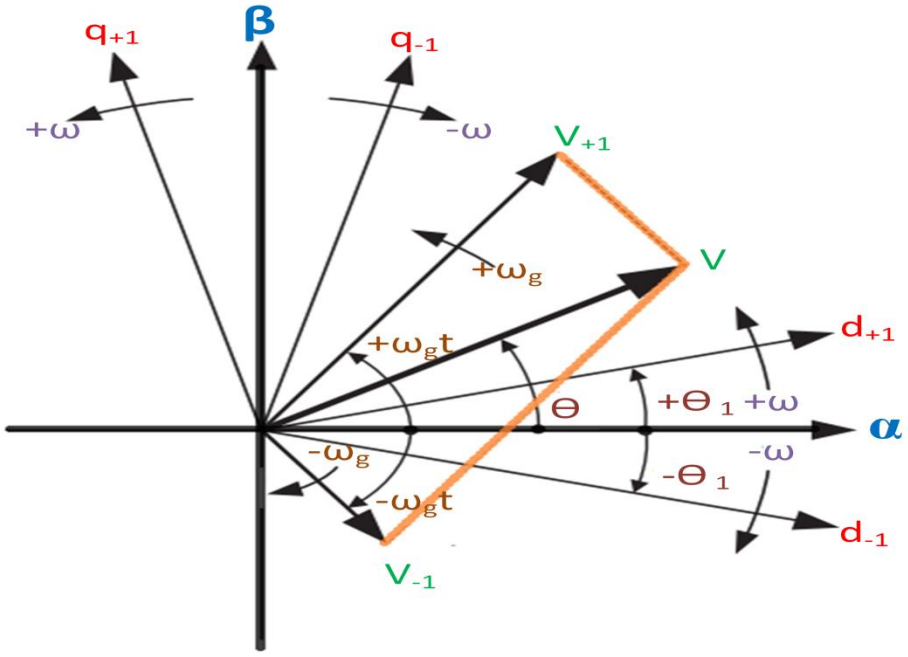


Figure 3- 11: Voltage vector on stationary and synchronous reference frame

It has also been found that any negative sequence component occurs twice frequently on the positive sequence rotational frame axis and vice versa, using Park's transform.

$$V_{dq+} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \sin(-\omega t) & \cos(\omega t) \end{bmatrix} \times \left[V_{+1} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t) \\ \sin(-\omega t) \end{bmatrix} \right] \tag{3.20}$$

$$= \left[V_{+1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} \right]$$

$$V_{dq-} = \begin{bmatrix} \cos(\omega t) & \sin(-\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \times \left[V_{+1} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t) \\ \sin(-\omega t) \end{bmatrix} \right] \tag{3.21}$$

$$= \left[V_{+1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} + V_{-1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \right]$$

This results in estimated errors for the phase angle of grid, which must be considered while design a phase locked loop for three phase utility attached applications.

The equations (3.20) and (3.21) demonstrate that the DC values upon that dq_+ and dq_- frames correspond to the amplitudes of the sinusoidal signals V_{+1} andV_{-1}, respectively, and that the oscillations at 2ω represent the coupling between axes caused by the voltage vectors rotary in opposite directions. Rather than employing any filtering approach to attenuate oscillations at 2ω, the next section presents a decoupling network that totally cancels out the influence of these kinds of oscillations on the PLL synchronous reference frame voltages.

3.2.2 Decoupling Network

The decoupling network employed in the DSRF can be explained in general terms by assuming a voltage vector with two generic components revolving at +ωt and +ωt frequencies, respectively. Thus, the voltage vector is given by this generic voltage vector.

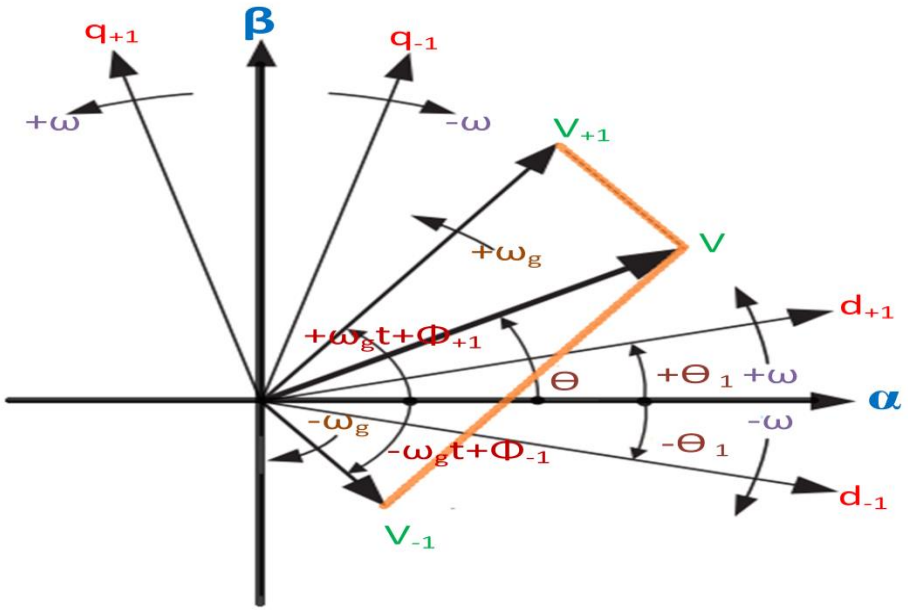


Figure 3- 12: Voltage vector representation

It is clear from (3.20) and (3.21) that AC amplitudes in dq_+ axes are directly proportional to DC amplitudes of signals in dq_- axes. Decoupling block can be designed to cancel out the oscillations generated by the negative sequence voltage vector(v_-)on dq_+ axes signals after identifying the coupling terms between both reference frames, as shown in the Figure 3-12. As a further consideration, two rotating reference frames, dq_+ and dq_- are examined. It is possible to represent the voltage vector as described as:

$$v = V_{+1}\begin{bmatrix}\cos(\omega t+\varphi_{+1})\\ \cos(\omega t-\frac{2\pi}{3}+\varphi_{+1})\\ \cos(\omega t-\frac{4\pi}{3}+\varphi_{+1})\end{bmatrix} + V_{-1}\begin{bmatrix}\cos(\omega t+\varphi_{-1})\\ \cos(\omega t-\frac{2\pi}{3}+\varphi_{-1})\\ \cos(\omega t-\frac{4\pi}{3}+\varphi_{-1})\end{bmatrix} + V_0\begin{bmatrix}1\\1\\1\end{bmatrix} \quad (3.21)$$

The simplification of voltage vectors of DDSRF-PLL are represented as:

$$v_{\alpha\beta} = \begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix} = v_{\alpha\beta_{+1}} + v_{\alpha\beta_{-1}} = V_{+1}\begin{bmatrix}\cos(\omega t+\varphi_{+1})\\ \sin(\omega t+\varphi_{-1})\end{bmatrix} + V_{-1}\begin{bmatrix}\cos(-\omega t+\varphi_{+1})\\ \sin(-\omega t+\varphi_{-1})\end{bmatrix} \quad (3.22)$$

$$v_{dq+} = \begin{bmatrix}v_{d+}\\ v_{q+}\end{bmatrix} = \begin{bmatrix}\bar{v}_{d+}\\ \bar{v}_{q+}\end{bmatrix} + \begin{bmatrix}\tilde{v}_{d+}\\ \tilde{v}_{q+}\end{bmatrix} \quad (3.23)$$

$$V_{dq+} = \begin{bmatrix}\cos(\omega t) & \sin(\omega t)\\ \sin(-\omega t) & \cos(\omega t)\end{bmatrix} \times V_{+1}\begin{bmatrix}\cos(\omega t+\varphi_{+1})\\ \sin(\omega t+\varphi_{-1})\end{bmatrix} + V_{-1}\begin{bmatrix}\cos(-\omega t+\varphi_{+1})\\ \sin(-\omega t+\varphi_{-1})\end{bmatrix}$$

$$= \left[V_{+1}\begin{bmatrix}\cos(\varphi_{+1})\\ \sin(\varphi_{+1})\end{bmatrix} + V_{-1}\begin{bmatrix}\cos(-\omega t+\varphi_{-1})\cos(\omega t)+\sin(-\omega t+\varphi_{-1})\sin(\omega t)\\ -\cos(-\omega t+\varphi_{-1})\sin(\omega t)+\sin(-\omega t+\varphi_{-1})\cos(\omega t)\end{bmatrix}\right] \quad (3.24)$$

$$V_{dq+} = \underbrace{V_{+1}\begin{bmatrix}\cos(\varphi_{+1})\\ \sin(\varphi_{+1})\end{bmatrix}}_{\text{DC Component}} + \underbrace{V_{-1}\begin{bmatrix}\cos(-2\omega t+\varphi_{-1})\\ \sin(-2\omega t+\varphi_{-1})\end{bmatrix}}_{\text{AC Component}} \quad (3.25)$$

$$V_{dq+} = \left[V_{+1}\begin{bmatrix}\cos(\varphi_{+1})\\ \sin(\varphi_{+1})\end{bmatrix} + V_{-1}\begin{bmatrix}\cos(\varphi_{-1})\cos(2\omega t)+\sin(\varphi_{-1})\sin(2\omega t)\\ \sin(\varphi_{-1})\cos(2\omega t)-\cos(\varphi_{-1})\sin(2\omega t)\end{bmatrix}\right] \quad (3.26)$$

$$V_{dq+} = \left[V_{+1}\begin{bmatrix}\cos(\varphi_{+1})\\ \sin(\varphi_{+1})\end{bmatrix} + V_{-1}\cos(\varphi_{-1})\begin{bmatrix}\cos(2\omega t)\\ -\sin(2\omega t)\end{bmatrix} + V_{-1}\sin(\varphi_{-1})\begin{bmatrix}\sin(2\omega t)\\ \cos(2\omega t)\end{bmatrix}\right]$$

$$V_{dq-} = \left[V_{-1}\begin{bmatrix}\cos(\varphi_{-1})\\ \sin(\varphi_{-1})\end{bmatrix} + V_{+1}\cos(\varphi_{+1})\begin{bmatrix}\cos(2\omega t)\\ \sin(2\omega t)\end{bmatrix} + V_{+1}\sin(\varphi_{+1})\begin{bmatrix}-\sin(2\omega t)\\ \cos(2\omega t)\end{bmatrix}\right] \quad (3.27)$$

$$v_{d+(\text{decouple})} = v_{d+} - (v_{d-}\times\cos(2\omega t)) - (v_{q-}\times\sin(2\omega t)) \quad (3.28)$$

$$v_{q+(\text{decouple})} = v_{q+} + (v_{d-}\times\sin(2\omega t)) + (v_{q-}\times\cos(2\omega t)) \quad (3.29)$$

3.2.3 Mathematical analysis of DDSRF-PLL

To better comprehend the DDSRF's performance during unbalanced grid disturbances, this part will describe a more intuitive analysis on the complex-frequency domain, which has been previously presented in reference [17]. The dq_+ and dq_- signals are re-written after rearranging equation (3.26) and equation (3.27).

$$v_{dq+} = \begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = V_{+1} \begin{bmatrix} \cos\varphi_{+1} \\ \sin\varphi_{+1} \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(2\omega t) & \sin(2\omega t) \\ -\sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos\varphi_{-1} \\ \sin\varphi_{-1} \end{bmatrix} \quad (3.30)$$

$$v_{dq-} = \begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} = V_{-1} \begin{bmatrix} \cos\varphi_{-1} \\ \sin\varphi_{-1} \end{bmatrix} + V_{+1} \begin{bmatrix} \cos(2\omega t) & -\sin(2\omega t) \\ \sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos\varphi_{+1} \\ \sin\varphi_{+1} \end{bmatrix} \quad (3.31)$$

It is evident from these equations that the AC terms in the $dq+$ axis arise as a result of a rotating transformation matrix at twice frequency having an effect on the DC terms in the $dq-$axes. It is possible to draw a similar result for AC signals in the reference frame of $dq-$.

Here, it is assumed that:

$$\left[M(2\omega)_{dq}\right] = \left[M(-2\omega)_{dq}\right]^T = \begin{bmatrix} \cos(2\omega t) & -\sin(2\omega t) \\ \sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \quad (3.32)$$

Hence, substituting equation (3.32) into the equations (3.30) and (3.31) and simplified equations are expressed as:

$$v_{dq+} = \begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = \bar{v}_{dq+} + \left[M(2\omega)_{dq}\right]\bar{v}_{dq-} \quad (3.33)$$

$$v_{dq-} = \begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} = \bar{v}_{dq-} + \left[M(-2\omega)_{dq}\right]\bar{v}_{dq+} \quad (3.34)$$

It corresponds to the amplitude of sequence components given to the DDSRF's input signal. In this manner, equations (3.33) and (3.34) demonstrate that the interrelationship between signals on the positive and negative coordinate systems is described by the equation.

Here, v_{dq+} and v_{dq-} are derived as:

$$\bar{v}_{dq+} = \begin{bmatrix} \bar{v}_{d+} \\ \bar{v}_{q+} \end{bmatrix} = V_{+1} \begin{bmatrix} \cos\varphi_{+1} \\ \sin\varphi_{+1} \end{bmatrix} \quad (3.35)$$

$$v_{dq-} = \begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} = V_{-1} \begin{bmatrix} \cos\varphi_{-1} \\ \sin\varphi_{-1} \end{bmatrix} \quad (3.36)$$

Here, equations (3.33) and (3.34) are rearranged as:

$$\bar{v}_{dq+} = (v_{dq+}) - \left[M(2\omega)_{dq}\right]\bar{v}_{dq-} \quad (3.37)$$

$$\bar{v}_{dq-} = (v_{dq-}) - \left[M(-2\omega)_{dq}\right]\bar{v}_{dq+} \tag{3.38}$$

Therefore, the computed component at the DDSRF's output can be expressed as follows:

$$\bar{v^*}_{dq+} = [K_{filter}]\{(v_{dq+}) - \left[M(2\omega)_{dq}\right]\bar{v^*}_{dq-}\} \tag{3.39}$$

$$\bar{v^*}_{dq-} = [K_{filter}]\{(v_{dq-}) - \left[M(-2\omega)_{dq}\right]\bar{v^*}_{dq+}\} \tag{3.40}$$

Here, $[K_{filter}]$ is nothing but either low-pass filter or moving average filter and transfer function of low-pass filter is defined as:

$$[K_{filter}] = \begin{bmatrix} \frac{\omega_k}{s+\omega_k} & 0 \\ 0 & \frac{\omega_k}{s+\omega_k} \end{bmatrix} \tag{3.41}$$

As a result, by substituting equation (3.32)and(3.41) into (3.35), it can be rewritten as

$$\bar{v^*}_{dq+} = [K_{filter}]\{(v_{dq+}) - (\left[M(2\omega)_{dq}\right][K_{filter}]\{(v_{dq-}) - \left[M(-2\omega)_{dq}\right]\bar{v^*}_{dq+}\})\} \tag{3.42}$$

By applying $v_{dq-} = \left[M(-2\omega)_{dq}\right]v_{dq+}$ and $v_{dq+} = \left[M(2\omega)_{dq}\right]v_{dq-}$ in equation (3.42), it is re-written as:

$$\bar{v^*}_{dq+} = [K_{filter}]\,(v_{dq+} - \{\left[M(2\omega)_{dq}\right][K_{filter}]\{\left[M(-2\omega)_{dq}\right]v_{dq+} - \left[M(-2\omega)_{dq}\right]\bar{v^*}_{dq+}\}) \tag{3.43}$$

$$\bar{v^*}_{dq+} = [K_{filter}] \times (v_{dq+} - \{\left[M(2\omega)_{dq}\right][K_{filter}]\left[M(-2\omega)_{dq}\right] \times \{v_{dq+} - \bar{v^*}_{dq+}\}) \tag{3.44}$$

For the simplicity,

$$[K] = \left[M(2\omega)_{dq}\right][K_{filter}]\left[M(-2\omega)_{dq}\right]$$

$$= \frac{1}{2}\begin{bmatrix} \frac{\omega_k(s+\omega_k)}{s^2+2s\omega_k+{\omega_k}^2+(2\omega)^2} & \frac{\omega_k\omega}{s^2+2s\omega_k+{\omega_k}^2+(2\omega)^2} \\ \frac{\omega_k\omega}{s^2+2s\omega_k+{\omega_k}^2+(2\omega)^2} & \frac{\omega_k(s+\omega_k)}{s^2+2s\omega_k+{\omega_k}^2+(2\omega)^2} \end{bmatrix} \tag{3.45}$$

Equation (3.45) is re-written as:

$$\bar{v^*}_{dq+} = [K_{filter}] \times (v_{dq+} - \{[K] \times \{v_{dq+} - \bar{v^*}_{dq+}\}) \tag{3.46}$$

The computed positive sequence component is describe as

$$\bar{v^*}_{dq+} = (\{[I] - [K][K_{filter}]\}^{-1} \times [K_{filter}]\{[I] - [K]\})v_{dq+} \tag{3.47}$$

The transfer function is expressed as:

$$\frac{\overline{v^*_{dq+}}}{v_{dq+}} = \begin{bmatrix} A & B \\ -B & A \end{bmatrix} \tag{3.48}$$

Here A and B are derived as:

$$A = \frac{\omega_k(s^3+2\omega_k s^2+4\omega^2 s+4\omega_k\omega^2)}{s^4+4\omega_k s^3+4(\omega_k^2+\omega^2)s^2+8\omega_k\omega^2 s+4\omega^2\omega_k^2} \; ; \; B = \frac{-\omega_k\omega_k\omega\, s}{s^4+4\omega_k s^3+4(\omega_k^2+\omega^2)s^2+8\omega_k\omega^2 s+4\omega^2\omega_k^2}$$

(a)

(b)

(c)

(d)

(e)

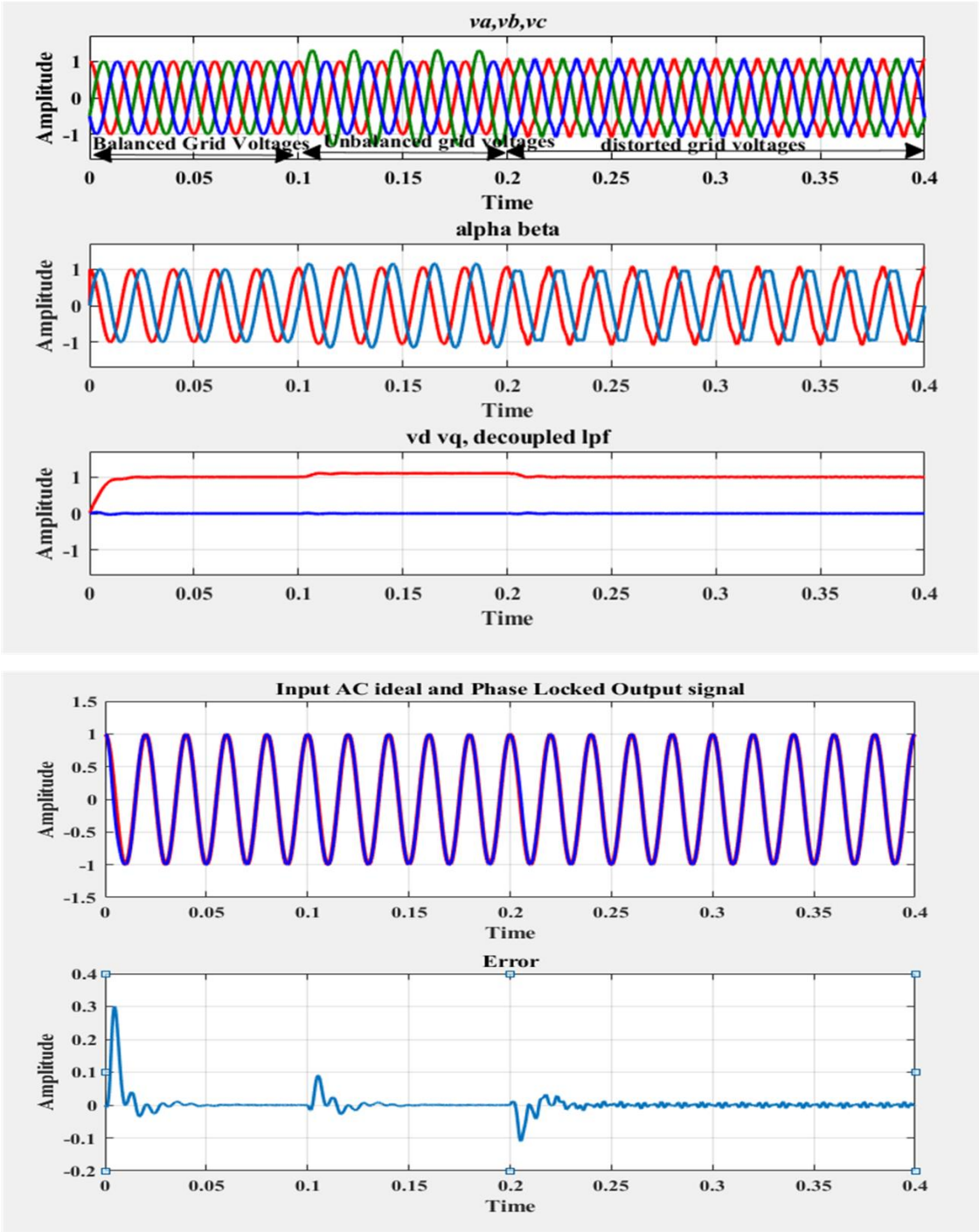


Figure 3- 13: Dynamic performance of DDSRF-PLL during balanced grid voltages, unbalanced in phase B of grid voltages, and distorted grid voltages

Figure 3-13 indicates the dynamic performance of DDSRF-PLL during balanced grid voltages till t = 0.1 second, further encounter to unbalance in Phase –B of grid voltages from t= 0.1 seconds to t =0.2 seconds, and further balance grid voltages distorted by harmonics from 0.2 seconds to t =0.3 seconds. The DDSRF-LL is used to extract phase-angle as well as positive sequences i.e.v_{α}^{+}, v_{β}^{+} (Figure 3-13 (b)) and both are used to generate v_d and v_q (see Figure 3-13 (c)) for the control system of grid connected system. Figure 3.13(d) shows phase-A of grid voltages and ac voltage generated using extracted phase- angle. The error signal is generated by computing difference between zeros and v_q^+ or multiplying gain of -1 to v_q^+ signal as per convenience. Figure 3-14 indicates the dynamic performance of DDSRF-PLL during balanced grid voltages till t = 0.1 second, further encounter to unbalance (i.e. swell) in Phase –B of grid voltages as well as distortion in grid voltages from t= 0.1 seconds to t =0.2 seconds, and further unbalance (i.e. sag) in phase-B of grid voltages distorted by harmonics from 0.2 seconds to t =0.3 seconds. The DDSRF-PLL is used to extract phase-angle as well as positive sequences i.e.v_{α}^{+}, v_{β}^{+} (Figure 3-14 (b)) and both are used to generate v_d and v_q (Figure 3-14 (c)) for the control system of grid connected system. To get a negative-sequence component and its transfer function, just transpose the matrix indicated in (3.48), similarly as for a positive-sequence DDSRF. Because it is a sequence separator, the DDSRF may be used to manage voltage and/or current in three-phase systems during unbalanced grid disturbances, making it a particularly useful for the control technique. The cut-off frequency (ω_k) of the low-pass filter is chosen at design time to achieve desired system performance. Setting $\omega_k = \omega/\sqrt{2}$ rad/s [17] provides an acceptable balance between temporal responsiveness and damping. An effective synchronization technique for three-phase power converter controllers, especially if they have low-voltage ride-through capabilities under unbalanced grid failures, can be achieved using the DDSRF-PLL. However, resonant controllers can also be used to create power converter controllers on the stationary reference frame. The most essential synchronization variable in this scenario is the grid frequency, not the grid voltage phase angle. As the grid frequency is a more stable variable than the grid phase angle, it is logical to assume that grid fault controllers based on grid frequency detection will show a more robust performance. Adaptive filters functioning with a stationary reference frame are used

in the next section i.e. second order generalized integrator –frequency lock loop to demonstrate a synchronization system suited for use with resonant controllers for three-phase converters.

(a)

(b)

(c)

(d)

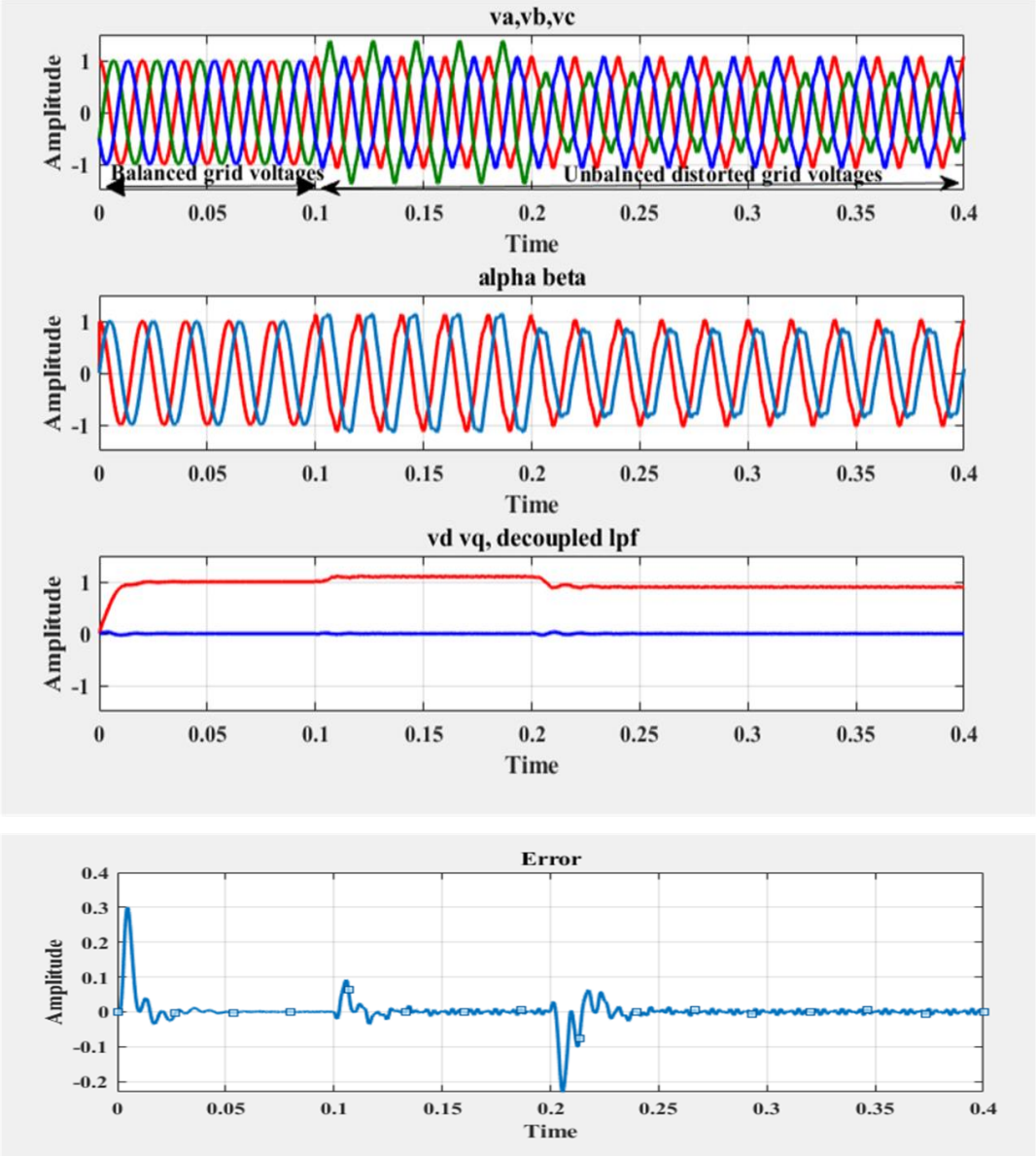


Figure 3- 14: Dynamic performance of DDSRF-PLL during balanced grid voltages, and unbalanced in phase B of distorted grid voltages

3.3 Dual Second-order generalized Integrator-FLL(DSOGI-FLL)

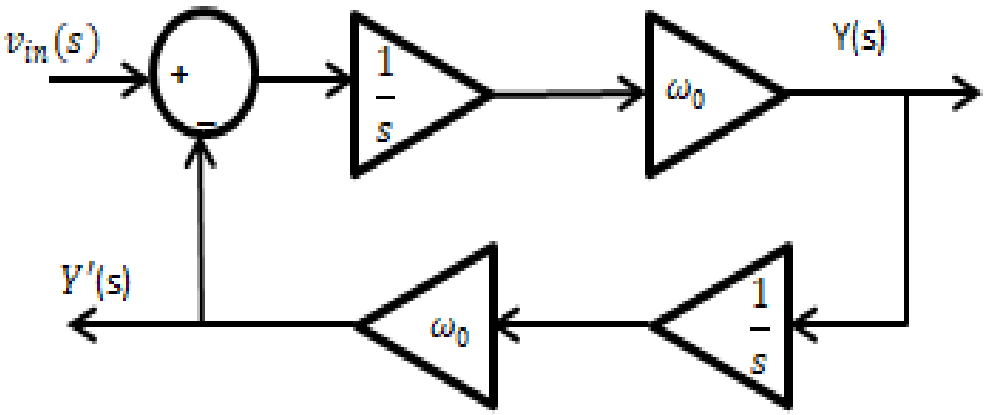
Our interest here is on a widely used enhanced PLL known as a DSOGI-PLL (dual second-order generalized integrator-phase locked loop). The DSOGI-PLL can be seen as a combo of the DSOGI and the traditional SRF-PLL entities to some extent. In order to avoid the negative and harmonic sequence during phase-angle extraction,

its primary principle of good performance against unbalanced grid voltage and harmonic distortion is able to deliver the pure, balanced, and sinusoidal grid voltage into the traditional SRF-PLL.

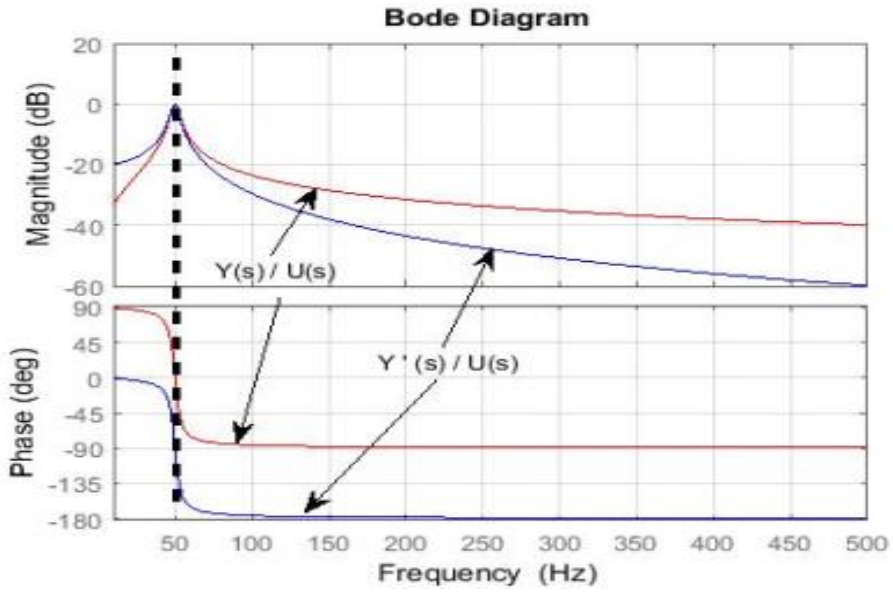
3.3.1 Second-Order Generalized Integrator (SOGI)

The second-order generalized integrator (SOGI), whose schematic diagram is illustrated in Figure 3-15, must be introduced before the DSOGI-PLL can be described. The structure of SOGI, as depicted in Figure 3-15, and the transfer function of SOGI in equations (3.49) and (3.50) are two imaginary complex conjugated poles located at $\pm j\omega_0$ that functioned like a resonator oscillating at angular frequency ω_0.

(a)



(b)



(c)

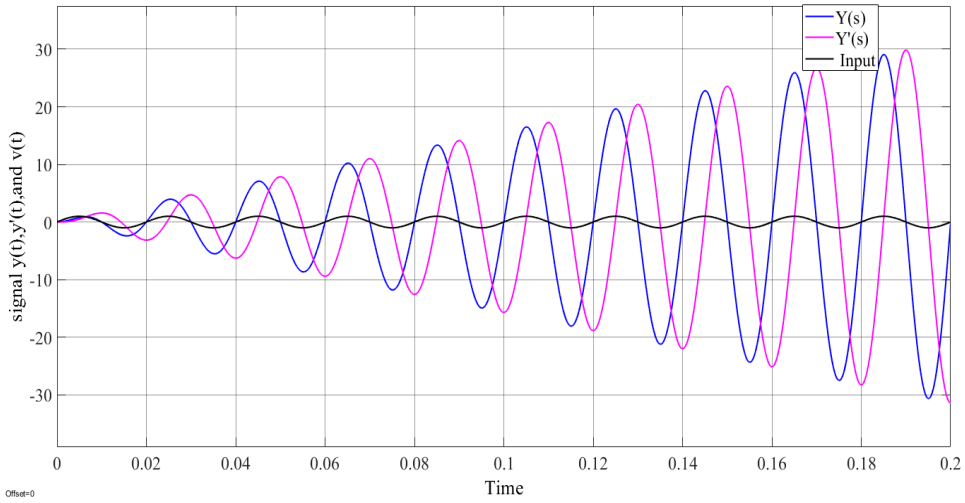


Figure 3- 15: (a) Basic structure of Second-order generalized integrator[11], (b) Bode diagram of transfer function (Y(s) / Vin (s))and (Y'(s) / Vin (s))of SOGI , and (c) Step response of SOGI

The transfer functions of SOGI from the Figure 3-15(a) are written as:

$$\frac{Y(s)}{v_{in}(s)} = \frac{\omega_0/_s}{1+\frac{\omega_0\omega_0}{s\ s}} = \frac{s\,\omega_0}{s^2+\ {\omega_0}^2} \tag{3.49}$$

$$\frac{Y'(s)}{v_{in}(s)} = \frac{Y'(s)}{Y(s)} * \frac{Y(s)}{v_{in}(s)} = \frac{\omega_0}{s} * \frac{s\,\omega_0}{s^2+\ {\omega_0}^2} = \frac{{\omega_0}^2}{s^2+\ {\omega_0}^2} \tag{3.50}$$

The step response of the SOGI is given as:

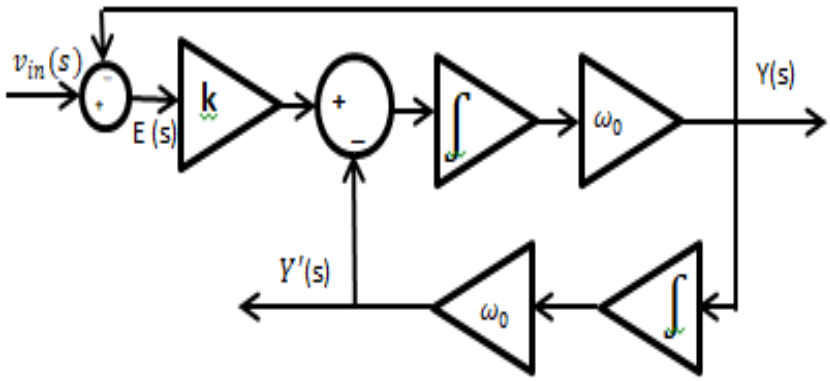
$$y\,(t) = L^{-1}[Y(s)] = L^{-1}\left[\frac{s\,\omega_0}{s^2+\ {\omega_0}^2} * v_{in}(s)\right] \tag{3.51}$$

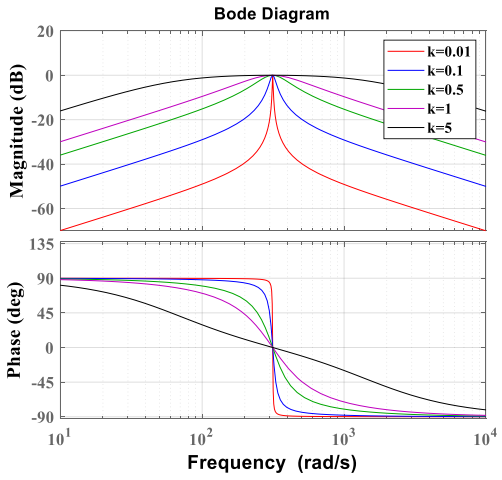
$$= L^{-1}\left[\frac{s\,\omega_0}{s^2+\ {\omega_0}^2} * \frac{\omega_0}{s^2+\ {\omega_0}^2}\right] = \frac{1}{2}[t\,\omega_0 \sin\omega_0 t]$$

$$y'(t)=L^{-1}[Y'(s)] = \frac{1}{2}[\sin\omega_0 t\ \ t\,\omega_0 \cos\omega_0 t] \tag{3.52}$$

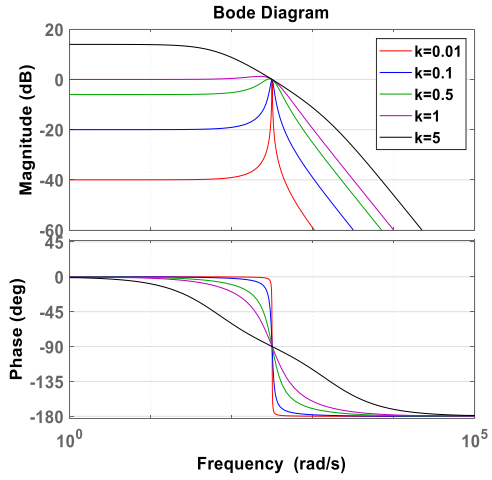
Figure 3-15 (c) depicts the step time response of a SOGI structure as a function of equations (3.51) and (3.52). In the presence of a unitary step, the amplitude of the output signals increases, resulting in an unstable system. Weighted k of the difference between grid voltage $v_{in}(s)$ and unity feedback of output signal Y(s), illustrated in Figure 3-16(a) is used to modify the input to the SOGI structure in order to prevent the system from being unstable.

(a)





(b)



(c)

Figure 3-16 :(a) Block diagram of SOGI-OSG, (b) Bode Diagram of $D_v(s)$, and (c) Bode Diagram of $Q_v(s)$with different value of k

The transfer functions for $D_v(s)$ and $Q_v(s)$ are rewritten as:

$$D_v(s) = \frac{Y(s)}{v_{in}(s)} = \frac{k\, s\, \omega_0}{s^2 + k\omega_0 s + {\omega_0}^2} \tag{3.53}$$

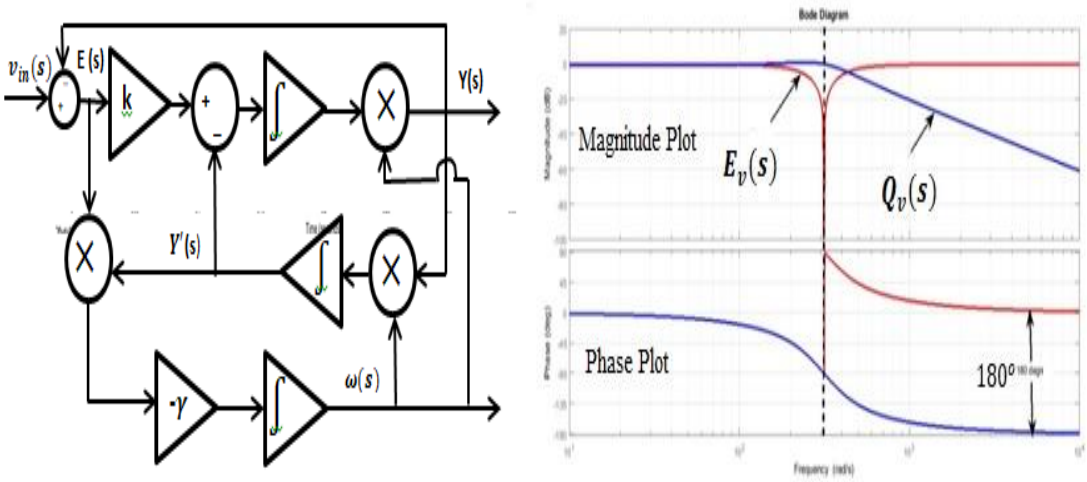
$$Q_v(s) = \frac{Y'(s)}{v_{in}(s)} = \frac{k\, s\, \omega_0}{s^2 + k\omega_0 s + {\omega_0}^2} \tag{3.54}$$

Figure 3-16 (b) indicates the band-pass equivalent nature of the output Y(s) and the low-pass similar nature of the output Y'(s)(Figure 3-16 (c)), while the phase responses of curves at 50Hz suggest that Y(s) is having a 90° phase lead to Y'(s). Furthermore, Bode's magnitude responses retain 0 dB level at the fundamental frequency of 50 Hz while decreasing the amplitude at the 5^{th} and 7^{th} harmonics harmonic frequencies of 250 Hz and 350 Hz, respectively. A second-order band-pass

filter is shown in Figure.3-16(b) to be capable of extracting only the fundamental components of utility grid yet rejecting harmonics.

3.3.2 Frequency Lock Loop (FLL)

However, SOGI has an intrinsic resonant nature that may be employed as a voltage-controlled oscillator, which stresses to create a simple and reliable single feedback control loop for an auto-adapting center frequency of SOGI resonator as per the input grid frequency.



(a) (b)

Figure 3-17: (a) Block diagram of SOGI-FLL, and (b) the Bode diagram of transfer functions, $E_v(s)$ and $Q_v(s)$(dotted line shows the SOGI resonance frequency (ω'))

Figure 3-17 shows a simple and reliable extension of the SOGI structure, which is Frequency Locked Loop, (FLL). The voltage error signal $E_v(s)$, which is nothing but the difference between input $v_{in}(s)$ and output Y(s) and behave as a notch filter with zero dB gain and a 180° phase-angle jump at the center frequency as observed from a bode diagram in the Figure 3-16, must be taken into consideration in order to make an auto-tunable SOGI-Quadrature Signal Generator (QSG) for single phase grid tied inverter.

Transfer function is expressed as:

$$E_v(s) = \frac{\varepsilon_{v(s)}}{V_{in(s)}} = \frac{s^2 + {\omega_0}^2}{s^2 + k\omega_0 s + {\omega_0}^2} \quad (3.50)$$

The transfer function of $E_v(s)$ and $Q_v(s)$ gives worthy information for auto-tunable frequency control system by taking common bode diagram of transfer function $E_v(s)$ and $Q_v(s)$, as depicted in Figure.3-17(b). The Bode diagram of transfer functions, $E_v(s)$ and$Q_v(s)$, reveal that the signals $E_v(s)$ and $Q_v(s)$ are in a phase when input frequency (ω) is lower than SOGI resonance frequency (ω') i.e. $\omega < \omega'$ and out of a phase (180^o phase difference) when $\omega > \omega'$, as indicated in the Figure.3-17(b).

Hence, a frequency error variable is derived from product of $E_v(s)$ and $Q_v(s)$, which remain positive when input frequency is lower than SOGI resonance frequency (ω'), and remain negative $\omega > \omega'$ in the SOGI-FLL. Moreover, the frequency-locking loop can be designed using frequency error variable, ε_f and a negative value of frequency loop controller gain,$-\gamma$ as shown in Figure 3-17 (a). The frequency loop controller gain is used to achieve DC component of frequency error variable ε_f equal to zero by changing SOGI resonance frequency, ω', until equal to the input frequency, ω. A feed-forward variable, ω_c i.e. nominal value of grid frequency is provided in frequency locking loop to speed up the initial synchronization process. The SOGI-QSG and Frequency locking loop combined structure diagram known as SOGI-FLL for single-phase grid synchronization system, as shown in Figure 3-17. The transient and steady state behavior of the SOGI –FLL mainly depends on a suitable value chosen for control parameters γ and k in order to obtain desired response in the estimation of the frequency and amplitude of input signal. Figure 3-16 shows two different transfer functions, k=0.1 and ω=100πrad/s, which we can consider second-order band-pass filters that can only retrieve AC signals propagating at the fundamental angular speed while excluding all other AC harmonics (for example, the fifth and seventh harmonic components). It is possible to eliminate harmonics by using a single SOGI for three phase system, and also generate quadrature signal for single phase system only, but the negative sequence will remain present in three phase system during abnormity in grid. Instead of single

SOGI, v_α andv_β signal applied to the two separate SOGI for the both signal. To eliminate harmonics and negative sequence from the v_α and v_β signal, two SOGI are used independently to form the direct/quadrature signal for v_α andv_β , which is referred to as the Dual-Second Order generalized integrator.

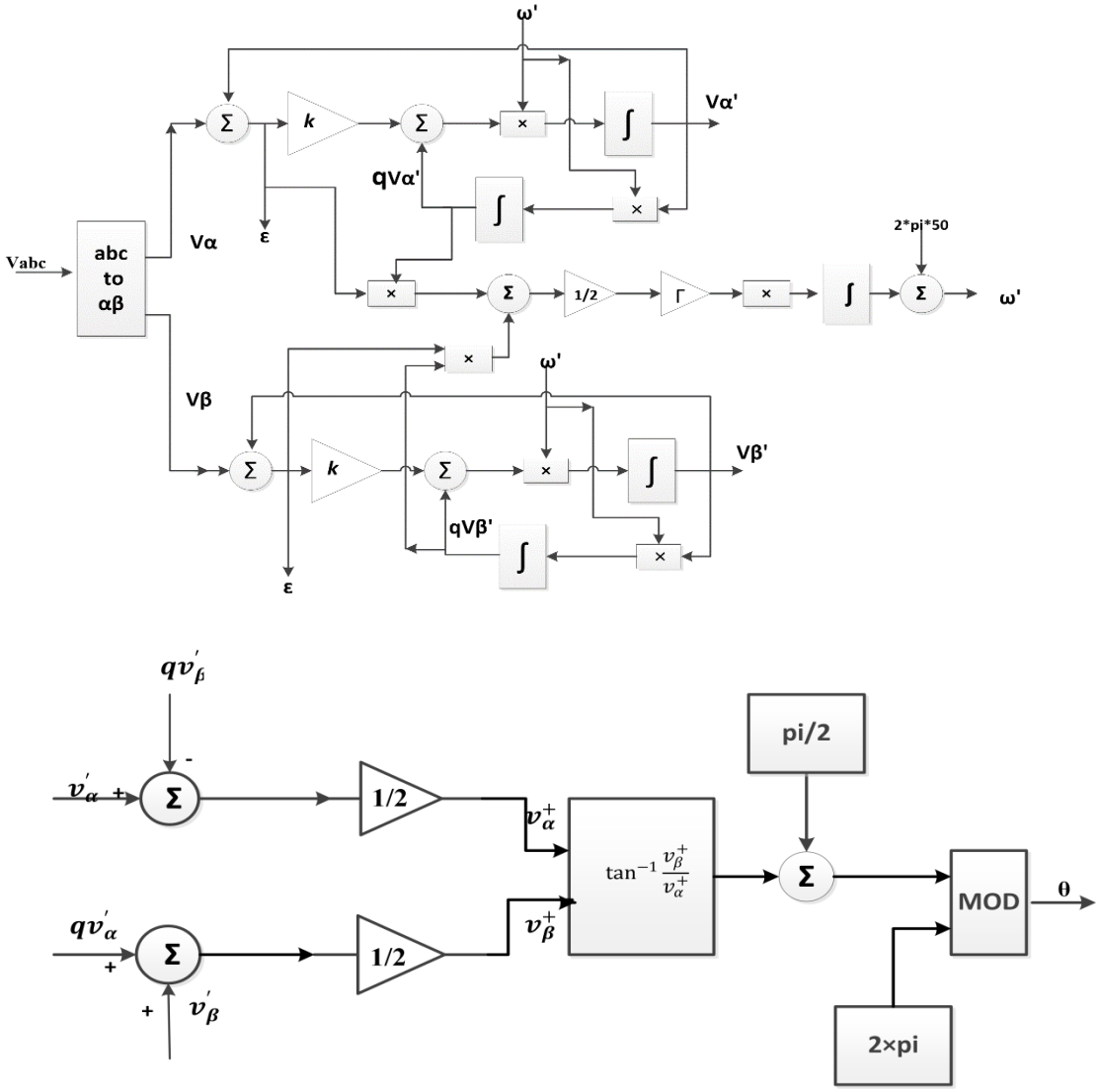


Figure 3-18: Schematic diagrams of the Dual SOGI and phase-angle computation

The functional diagram shown in Figure 3-18 illustrates a dual-second order generalized integrator (DSOGI) in association with a frequency lock loop (FLL) and tangent-based phase-angle computation block. Figure 3-19 depicts a four-phasor diagram, with the first and second phasor diagrams representing the positive direct/quadrature components of v_α and v_β, respectively, and the third and fourth

phasor diagrams representing the negative direct/quadrature components of v_α and v_β, respectively.

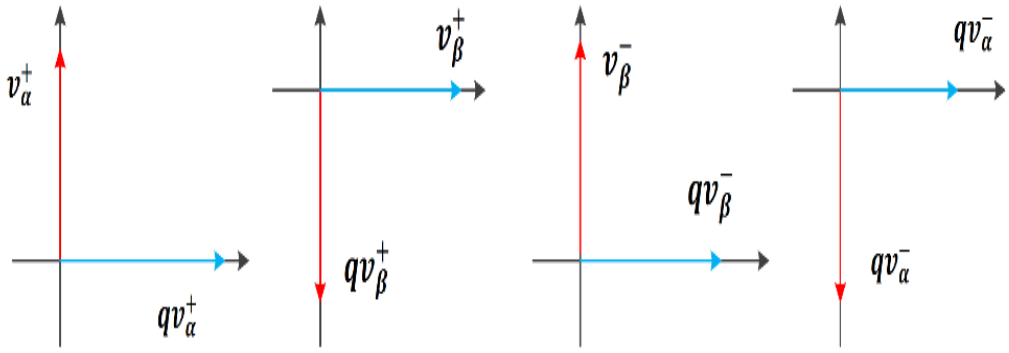


Figure 3-19:Phasor diagram of direct/quadrature components of v_α and v_β grid voltage

As seen in Figure 3-16, the direct component is 90^ophase leading phase leading in relation to the quadrature components, whereas the negative component rotates in the opposite direction of -50Hz.

From Figure 3-18 and Figure 3-19, following result are obtained ($v'_{\alpha+} = (- qv'_{\beta+})$ and $v'_{\beta+} = (-qv'_{\alpha+}))$ as:

$$v'_\alpha - qv'_\beta = (v'_{\alpha+} + v'_{\alpha-}) - (qv'_{\beta+} + qv'_{\beta-}) = v'_{\alpha+} - qv'_{\beta+} = 2v'_{\alpha+} \quad (3.51)$$

$$qv'_\alpha + v'_\beta = (qv'_{\alpha+} + qv'_{\alpha-}) + (v'_{\beta+} + v'_{\beta-}) = qv'_{\alpha+} - qv'_{\beta+} = 2v'_\beta \quad (3.52)$$

$$\varepsilon_f = \frac{\varepsilon_{f(\alpha)} + \varepsilon_{f(\beta)}}{2} = \frac{1}{2}(\varepsilon_\alpha qv'_\alpha + \varepsilon_\beta qv'_\beta) \quad (3.53)$$

In SOGI-QSG, a frequency adaptive FLL is included to achieve grid synchronization in a changing frequency environment. Additionally, the normalized gain of the FLL is calculated by dividing the amplitude of positive sequence components by two, i.e. $(v_\alpha^+)^2 + (v_\beta^+)^2$, in order to linearize the frequency lock loop response. While technically valid, the usage of two separate FLLs in the DSOGI-FLL may seem unusual conceptually due to the fact that its two input signals have the same frequency. Due to the fact that both inputs, $v_\alpha$and v_β, have the same frequency, the DSOGI employs a single FLL (Figure 3-18) in which the frequency error signals created by calculating an average error signal, i.e. . $\varepsilon_{f(\alpha)}$ and $\varepsilon_{f(\beta)}$ of the QSGs, have been combined in the equation (3.53).

The state-space equations of DSOGI can be written as:

$$\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix} = \frac{1}{2} * \begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{1}{2} * \frac{k\times\omega'}{s^2 + k\times\omega'\times s + \omega'^2} \begin{bmatrix} s & -\omega' \\ -\omega' & s \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (3.54)$$

The frequency response of the DSOGI can be described as

$$\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix} = \frac{1}{2} * \frac{k\times\omega'}{k\times\omega\times\omega' - j(\omega^2 + \omega'^2)} \begin{bmatrix} j\omega & -\omega' \\ -\omega' & j\omega \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (3.55)$$

Assuming balanced positive-sequence voltage vector at the grid frequency, steady-state analysis gives following relationship:

$$v_\beta(s) = -j\, v_\alpha(s) \quad (3.56)$$

Hence, the Steady-state frequency response of the DSOGI is re-written as:

$$\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix} = \frac{1}{2} * \frac{k\times\omega'(\omega' + \omega)}{k\times\omega\times\omega' - j(\omega^2 + \omega'^2)} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (3.57)$$

The transfer functions gives the relation between the amplitude of the positive sequence component detected by the DSOGI and the actual amplitude of a given positive sequence voltage vector applied to its input. The transfer function $\frac{|v_{\alpha\beta}^{+\prime}|}{|v_{\alpha\beta}^-|}$ obtained by substituting ω by –ω. The bode plot of transfer function is shown in Figure 3-20.

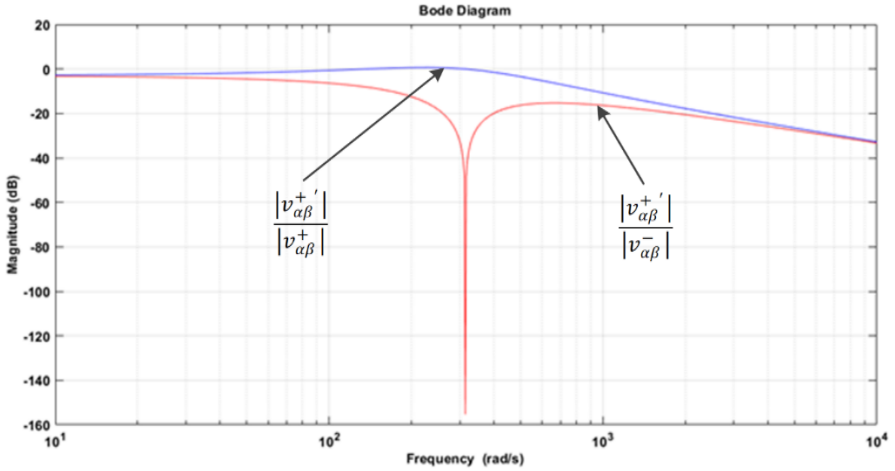


Figure 3-20: Bode plot of transfer functions $\frac{|v_{\alpha\beta}^{+\prime}|}{|v_{\alpha\beta}^+|}$ and $\frac{|v_{\alpha\beta}^{+\prime}|}{|v_{\alpha\beta}^-|}$ in the Dual- SOGI

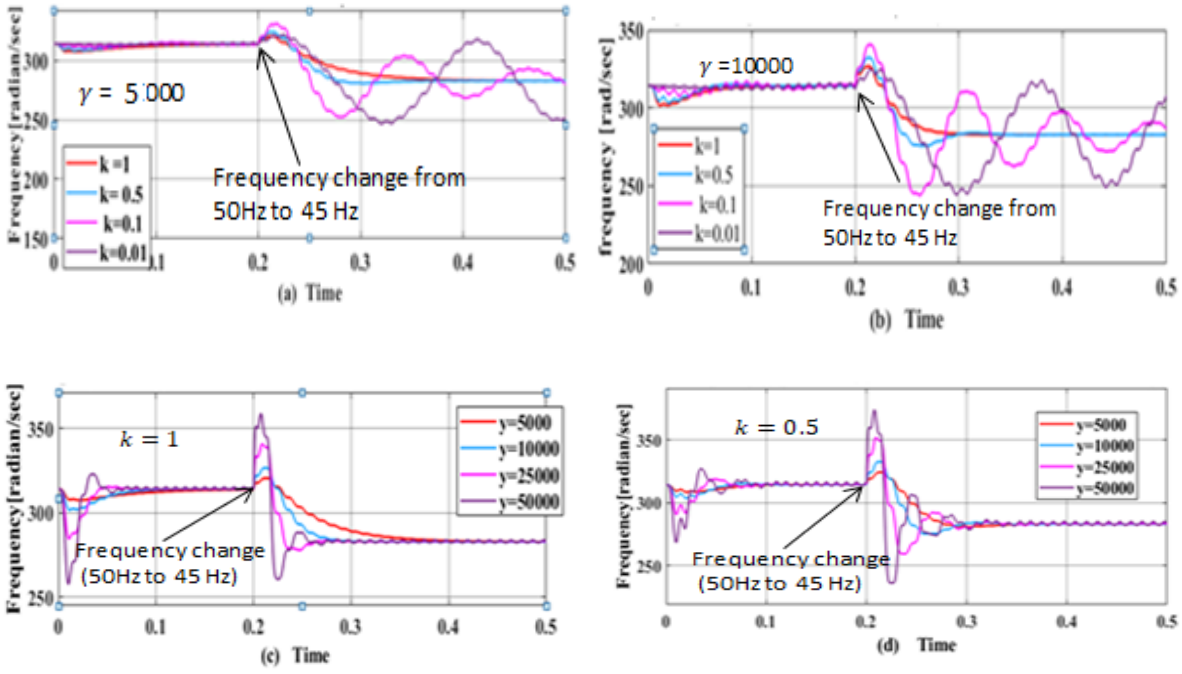


Figure 3-21 :Step response of Frequency Estimation (a) different value of k ,constant value γ=5000, (b) different value of k ,constant value γ=10000, (c) different value of γ ,constant value k=1, and (d) different value of γ ,constant value k=0.5

In spite of this, it is difficult to determine the advantages and disadvantages of these structures, particularly in contrast with the SOGI-FLL and high-order PLLs. The high-order PLLs and FLLs knowledge provides fast and accurate phase angle extraction by paying cost of hardware implementation complexity. Using a -5 Hz frequency step change (i.e. frequency leap (50Hz to 45Hz) and phase angle shift (0^0 to45^0) at 200msec, the dynamic performance of frequency estimation in SOGI-FLL is investigated. The starting frequency value, i.e. $2\pi * 50$, is used as the feed-forward value. The dynamic response of frequency estimation is observed in the Figures 3-21 (a) and (b) by taking a progressive value of k and a constant value of γ, while the dynamic response of frequency estimation is observed by taking a progressive value of γ and a constant value of k, as depicted in the Figures 3-21(c) and (d). The table 3-1contains the results of an impact study of the parameters k and γ in SOGI-FLL based on the Figures 3-21 (a)-(d) of the figure. Amplification of the signal (ε_v) is accomplished by the use of the parameter k, which has an effect on the transient responsiveness and bandwidth of SOGI-FLL. A good signal filtering performance

and a dynamic response of the system are compromised while choosing the gain k for the system (Figure.3-17 & Figure 3-21). It is necessary to choose a value that represents a trade-off between the precision of frequency estimate and the dynamics of SOGI-FLL.

Table 3-1: Impact Analysis of SOGI-FLL

Parameter	Progressive change	Transient response	Steady-state response	Filtering	Settling Time
k	Increasing	Good	Good	Good	Reduce
	Decreasing	Poor	Poor	Poor	Increase
γ	Increasing	Poor	moderate	No effect	Reduce
	Decreasing	Good	Good	No effect	Increase

The applicability of DSOGI-FLL is demonstrated by simulation results obtained in the MATLAB/Simulink programming environment. These are the control variables that are utilized in the simulation model: k= 1, $\gamma = -2000$. To achieve the simulation findings, four situations were considered, which are as follows: (i) balanced grid voltages; (ii) unbalanced sag in grid voltage; (iii) unbalanced swell in grid voltage; and (iv) harmonic distorted grid voltage. Figure 3-22 (a) depicts the situation I in which balanced three phase grid voltages are provided to DSOGI-FLL for a period of time equal to 0.1 seconds. Following that, voltage sag and swell are introduced into the phase A of grid voltage from t = 0.1 seconds to t= 0.15 seconds and from t = 0.15 seconds to t=2.0 seconds, respectively, in the phase A of grid voltages. This block is critical in the design and implementation of a control system for a grid-connected converter because it allows the converter to be synchronized with the grid. The v_d and v_q are generated for the control system of grid-connected systems using the dq-abc transformation and DSOGI-FLL, which is employed to extract phase-angle as well as positive sequences, i.e. v_α^+ and v_β^+, and both are utilised to generate v_d and $v_q$for the control system of grid-connected systems. DSOGI-band-pass FLL filtering capabilities are demonstrated in Figure 3-22(b), which depicts positive sequences of grid voltages (v_α^+ and v_β^+, FLL) that are devoid of the effects of sag, swell, and harmonics distortion, and which also confirms the

band-pass filtering capabilities of DSOGI-FLL. Figure 3-22(c) depicts the synchronism of grid voltages and phase-angle retrieved using DSOGI-FLL when all simulation situations are taken into consideration.

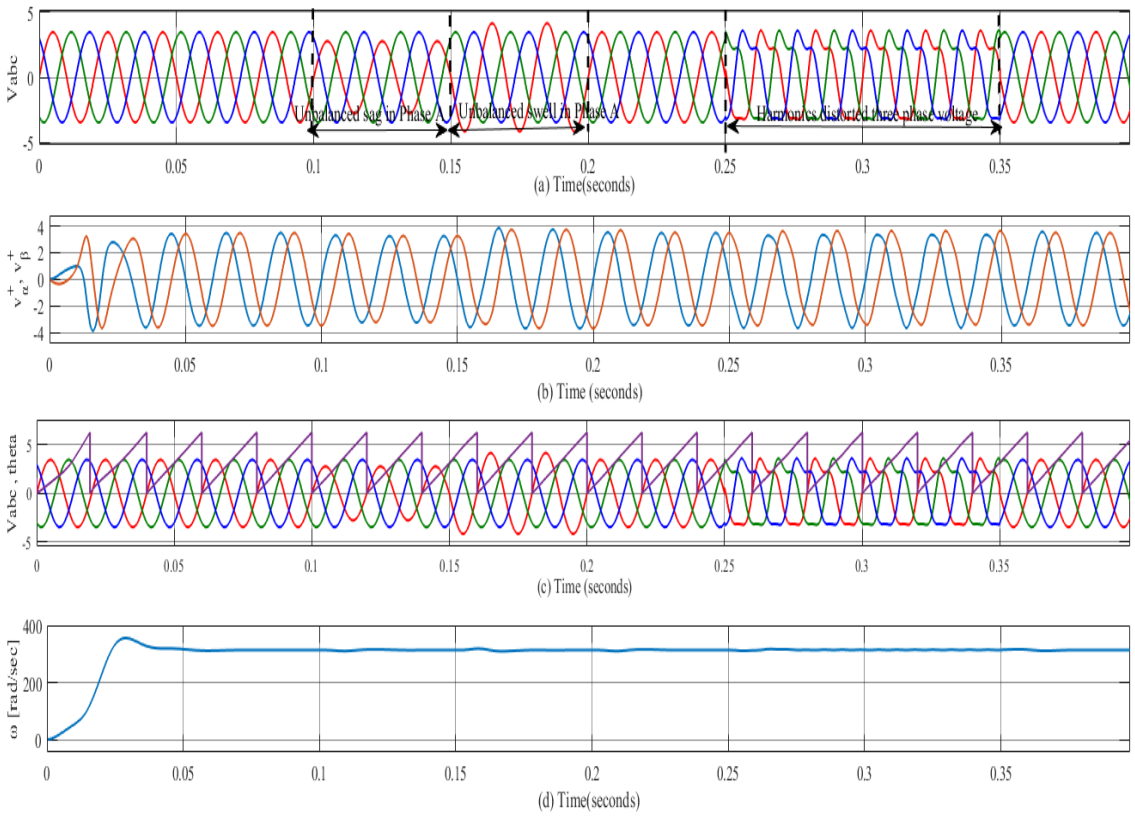


Figure 3-22. Simulation result of grid connected PV inverter using dual-SOGI-FLL :(a)PCC voltages with grid abnormalities,(b)positive component of stationary frame voltages, (c)comparative results of phase-angle and PCC voltages, and (d)frequency extraction

According to Figure 3-22 (d), the transient response of estimated frequency in DSOGI-FLL does not show any fluctuation or minimum change at the time in which either sag or swell encounter in the three-phase voltages and swiftly settles down to the desired value after settling down to the desired value. Figure 3-23 gives the comparative analysis of frequency extraction of different grid synchronization techniques when subjected frequency shifted from 50Hz to 45 Hz at the t= 0.25 seconds. The dynamic parameters are chosen for analysis as follow: $\omega_n = 2\pi 50$ rad/s, $\zeta = 0.707$.Table 3-2 presents settling time of frequency extraction, negative Sequence Components detection, and harmonics detection for the different grid

synchronization techniques. Hence, DSOGI-FLL gives superior performance over the other grid synchronization techniques.

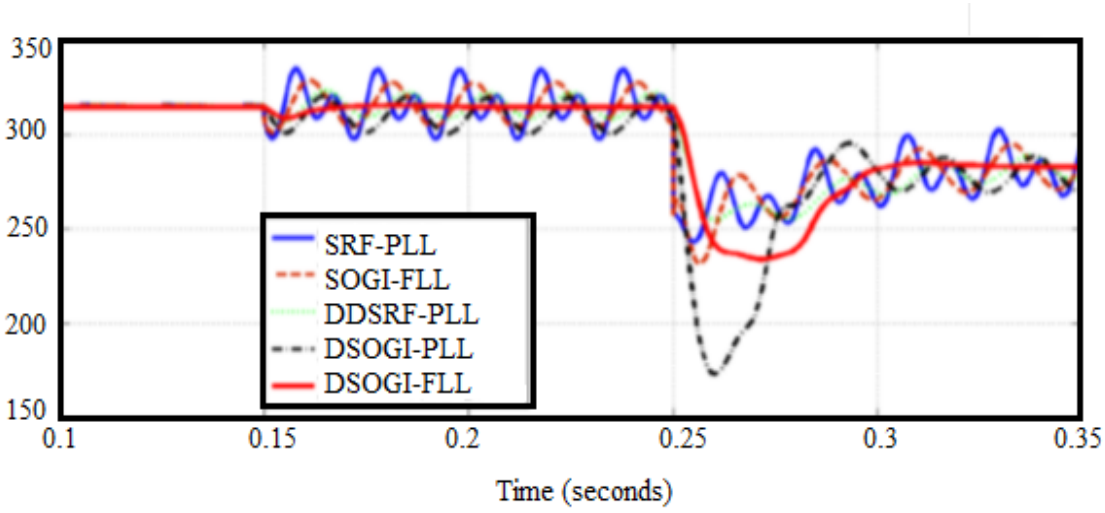


Figure 3-23: Time responses of frequency extraction in different grid synchronization techniques

Table 3-2: Time response of frequency extraction and performance assessment of different grid synchronization techniques.

Different grid synchronization techniques	Observed Time (ms)	Negative Sequence Components detection	Harmonics Detection
SRF-PLL	60	NO	NO
SOGI-FLL	54	NO	YES
DDSRF-PLL	50	YES	Required decoupling term
DSOGI-PLL	50	YES	YES
DSOGI-FLL	35	YES	YES

An FLL is used to adaptively obtain frequencies in SOGI-FLL, whereas the SOGI-PLL uses a SOGI-OSG block to provide feedback on the estimated frequency [6]. [15-18]. When the power grid fails, a DC-offset is produced by a variety of factors, including transformer nonlinearity, A/D converter error, abnormal temperature in

analogue devices, and zero drift[7-8]. The DC-offset in SRF-PLL can be reduced using a variety of methods. Cascaded-SOGI-PLL was recommended in the article [9] as a way to eliminate the DC quantity, although it has several drawbacks, such as segregation. The DC-offset in SRF-PLL can be reduced in a number of methods, including a cascaded SOGI-PLL, which uses many SOGI structures, although the additional computational cost is significant [10]. Cascade delay signal cancellation PLL (CDSC-PLL) and adaptive filter delay signal cancellation-PLL (APF-DSC-PLL) techniques were devised by the authors of an article [10] and an article [11], respectively, to speed up DC-offset removal. However, the complex structure of the system reduces the dynamic performance of the system. It was also reported in an article [12] that a PLL using modified delay signal cancellation-PLL can improve dynamic performance by minimizing DC-offset but requires design modification. As well as five more methods for removing the DC-offset in the PLL (NF) based on PLL and dq-DSC-PLL. However, the dynamic performance of these phase detection approaches is sluggish (articles [13-15]). While conventional low-pass filters have their limitations, these new techniques have the potential to improve dynamic performance while overcoming those drawbacks. Even so, the process of selecting and calculating the sliding window's width might be time-consuming. For single-phase or three-phase systems, a modified SOGI-FLL (MSOGI-FLL) is recommended to reduce frequency estimate errors due to DC quantity and other grid irregularities. Consequently (e.g. harmonics, frequency fluctuation, magnitude variation), MSOGI-FLL estimates the DC-offset by using the third integrator as a DC-offset cancellation block, which does not affect frequency estimation in the FLL. Under various circumstances, it is described how the MSOGI-FLL gives superior performance over other higher ordered FLL or PLL techniques without increasing computation burden.

3.3.2.1 DC-offset effect in SOGI-FLL

A DC-offset is produced by a variety of factors, including transformer nonlinearity, A/D converter error, and nonlinearity of op-amp in current or voltage sensor circuitry, abnormal temperature in analogue devices, and zero drift. One of the phase voltages of three phase system or alpha or beta voltage component including DC-offset, which has amplitude V_0 are expressed as:

$$v_{in}(t)\{or v_{\alpha}(t) or\ v_{\beta}(t)\} = V_0\, u(t) + V_1 \sin \omega t \tag{3.58}$$

The frequency transformation of the equation (3.58) can be described as:

$$v_{in}(s) = \frac{V_0}{s} + \frac{V_1\omega}{s^2+\omega^2} = \frac{V_0\left(s+\frac{V_1}{V_0}\omega+\frac{\omega^2}{s}\right)}{s^2+\omega^2} \tag{3.59}$$

From the block diagram of SOGI-FLL and equation (3.50), transfer function of error signal in SOGI-FLL can be expressed as:

$$\frac{E_v(s)}{v_{in}(s)} = \frac{s^2+\omega^2}{s^2+k\omega s+\omega^2} \tag{3.60}$$

$$E_v(s) = \frac{s^2+\omega^2}{s^2+k\omega s+\omega^2}\, v_{in}(s) = \frac{s^2+\omega^2}{s^2+k\omega s+\omega^2}\, \frac{V_0\left(s+\frac{V_1}{V_0}\omega+\frac{\omega^2}{s}\right)}{s^2+\omega^2} \tag{3.61}$$

$$= \frac{s^2+\omega^2}{s^2+k\omega s+\omega^2}\, \frac{V_0\times\frac{1}{s}\times\left(s^2+\frac{V_1}{V_0}\omega s+\frac{\omega^2}{s}\right)}{s^2+\omega^2} = \frac{V_0}{s}$$

The error signal in time domain can describe as:

$$e_v(t) = V_0\, u(t) \tag{3.62}$$

As a parameter of the resonance frequency, the SOGI system has to be constantly updated to keep it in sync. Continuous-to-discrete transformations in practical applications are required for the real-time calculation of coefficients. A major drawback of SOGI-FLL is that it is unstable if the input signal has a DC component. A high-pass filter should be applied to the input signal to eliminate DC-offset.

3.3.3 DC-offset due to Analog to Digital Conversion (ADC)

The DC-offset presents due to the analog to digital conversion(ADCs) and signal conditioning and the SOGI structure is inefficient to eliminate the DC-offset as observed from the bode diagram, shown in Figure 3-16(b). Bode diagram of the SOGI presents the inability to attenuate low-frequency components especially the dc signal from the grid voltage. It is very well common that integration of DC value yields step signal, further integration produces a ramp signal. Because of the analogue to digital conversion (ADCs) and signal conditioning, a DC-offset is introduced, and the SOGI structure is inefficient in eliminating the DC-offset, as per the previous derivation and equation (3.62). Because of this inability to attenuate low-frequency components, particularly DC signals from the grid voltage, the SOGI's Bode curve is shown in Figure 3-16. The existence of a DC-offset in the measured grid voltage degrades the performance of a SOGI by reducing its efficiency. The conversion of a continuous-time input signal into digital values results in the generation of an error, which is referred to as the quantization error.

This error occurs as a result of the ADC conversion process increasing the number of digits in the input signal by a set number of digits. If a normalized sinusoidal signal (i.e., one whose amplitude changes between +1 and -1) is to be converted into a digital ADC, (b+1) bits, including sign bits, must be used in the conversion. The number of levels and the size of the quantization step are 2^{b+1} and $\frac{2}{2^{b+1}} = 2^{-b}$ for the b+1 level, respectively. The quantization error is caused by rounding, which is the process of reducing the size of a binary number with a finite word size of b bits so that the rounded b-bit number is as close as possible to the original un-quantized input signal. Rounding is performed on binary numbers with a finite word size of b bits. The quantization error, denoted by the letter $e(n)$ is given by

$$e(n) = x_q(n) - x(n) \quad ; \quad x_q(n) = x(n) + e(n); \tag{3.63}$$

Where $x_q(n)$ and $x(n)$ are the sampled quantized value and the sample un-quantized value of the input signal to the ADCs respectively. Due to the rounding, the error signal obeys the following relations: $\frac{-q}{2} \leq e(n) \geq \frac{q}{2}$. In signal processing, a quantization error is commonly viewed as an unwanted discrete noise signal. Therefore, the output signal from the ADC is the sum of input signal $x(n)$ and error signal $e(n)$ as described in equation (8). The variance or power of the error signal $e(n)$ is given by:

$$\sigma_e^2 = \{E(e^2(n))\} - \{E^2(e(n))\} = \left\{\frac{q^2}{12} - (0)\right\} = \frac{2^{-2b}}{12} \tag{3.64}$$

Here, $E(e(n))$ is the mean value of $e(n)$ and its zero while $E(e^2(n))$ is the average value of $e^2(n)$ and $p(e)$ is the probability density function.

The average value of $e^2(n)$ is mathematically described as:

$$E(e^2(n)) = \int_{-\infty}^{\infty} e^2(n)\, p(e)\, de = \frac{1}{q}\int_{-q/2}^{q/2} e^2(n)\, de = \frac{q^2}{12};$$
$$p(e) = \frac{1}{q} \quad \text{for } \frac{-q}{2} \leq e(n) \leq \frac{q}{2} \tag{3.65}$$

The output signal of an ADC converter is passed through a first-order filter and described by:

$$y(n) = ay(n-1) + x(n) \tag{3.66}$$

Besides, the transfer function of the system and impulse response of the system is given as:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{z}{z-a}; \quad h(n) = a^n u(n) \tag{3.67}$$

The steady-state variance of a noise or quantization noise presents in the input signal is given as:

$$\sigma_\varepsilon^2 = \sigma_e^2 \sum_{k=0}^{\infty} h(n)^2 = \sigma_e^2 \left[\frac{1}{1-a^2}\right] = \frac{2^{-2b}}{12}\left[\frac{1}{1-a^2}\right] \tag{3.68}$$

Generally, digital signal processors have 10-bit or 12-bit ADCs. To eliminate the steady-state variance or quantization noise in the input signal, value of 'a' is preferably chosen from the range $0.5 \leq a \leq 0.99$ (ideally a lies between 0 <a<1 to remain Region of convergence (ROC) inside the unit circle for the stability).Assume a=0.98 and 12-bit digital signal processor, the quantization noise at the output of the filter is 4.2088e-22≈ 0.

3.3.3.1 IIR Filter for DC-offset elimination

The IIR based high pass filter is employed to eliminate DC-offset from sensed voltage/ current signals. Job of sensor card is to sense as well as scale the signal within range of digital signal processor (0 to 3.3 V). The digital signal processor have unipolar analog to digital converter, therefore, ac voltage/current signal must be converted from bipolar (i.e. -1.5 to +1.5 volt) to unipolar (i.e.0 to 3V) by adding offset value of 1.5V in hardware using analog electronics circuit (using op-amp).The block diagram of IIR based high pass filter is depicted in the Figure 3-24.

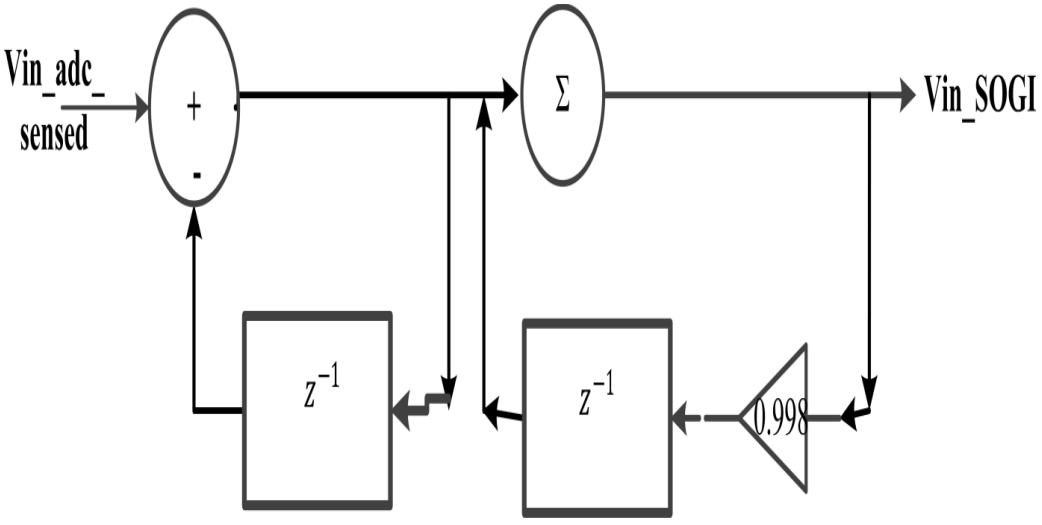


Figure 3-24: DC-offset elimination IIR high-pass Filter

The difference equations of IIR filter are described as:

$$x'(n) = x(n) - x'(n-1) \quad ; \quad y(n) = x'(n) + ky(n-1) \tag{3.69}$$

The Z-transform of the above difference equations are expressed as:

$$\frac{X\prime(Z)}{X(Z)} = \frac{1}{1+Z^{-1}} \quad ; \quad \frac{Y(Z)}{X\prime(Z)} = \frac{1}{1-kZ^{-1}} \tag{3.70}$$

The transfer function of IIR filter is defined as:

$$\frac{Y(Z)}{X(Z)} = \frac{Y(Z)}{X\prime(Z)} \; \frac{X\prime(Z)}{X(Z)} = \frac{1}{1-kZ^{-1}} \tag{3.71}$$

$$\frac{1}{1+Z^{-1}} = \frac{1}{1+Z^{-1}-kZ^{-1}-kZ^{-2}} = \frac{1}{1+(1-k)Z^{-1}-kZ^{-2}}$$

By applying inverse Z-transform, the difference equation can be described as:

$$y(n) = -(1+k)y(n-1)+ky(n-2) + x(n) \tag{3.72}$$

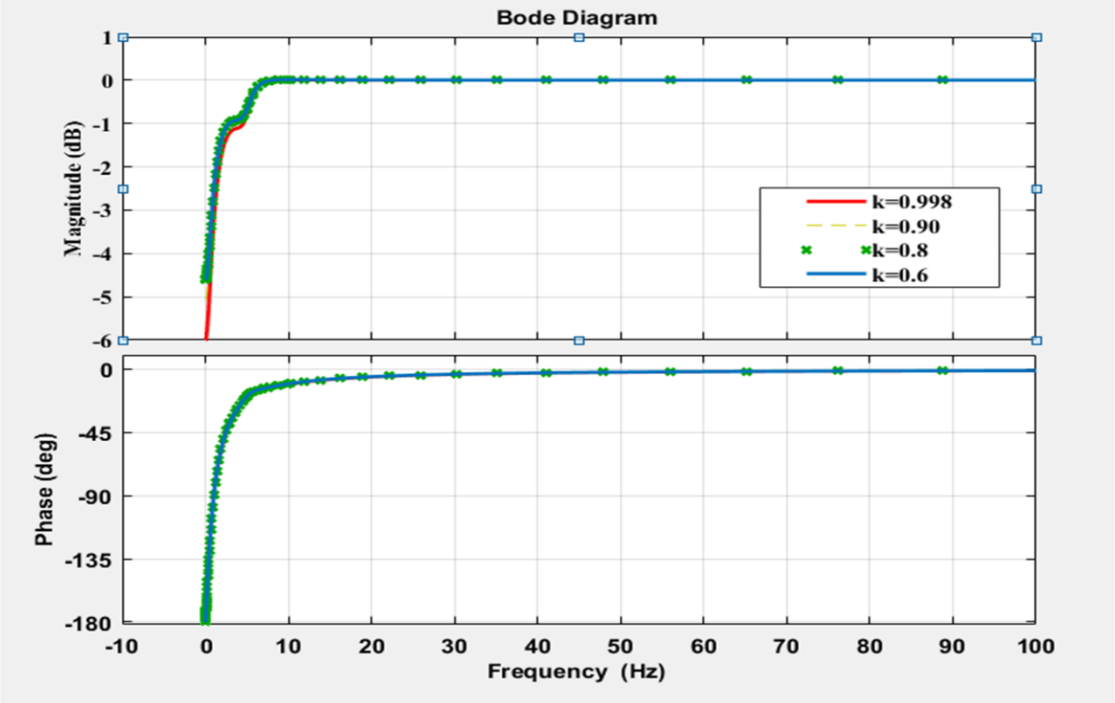


Figure 3-25: Bode plot of IIR high pass filter by taking different value of k

Bode diagram gives information regarding selection of value for parameter k. The value of parameter k for IIR high pass filter should be selected between 0.85 to 0.99, as shown in bode diagram 3-25.

3.4 Modified –Second order generalized Integrator – FLL

The fundamental structure of the SOGI-FLL is depicted in Figure 3-16.

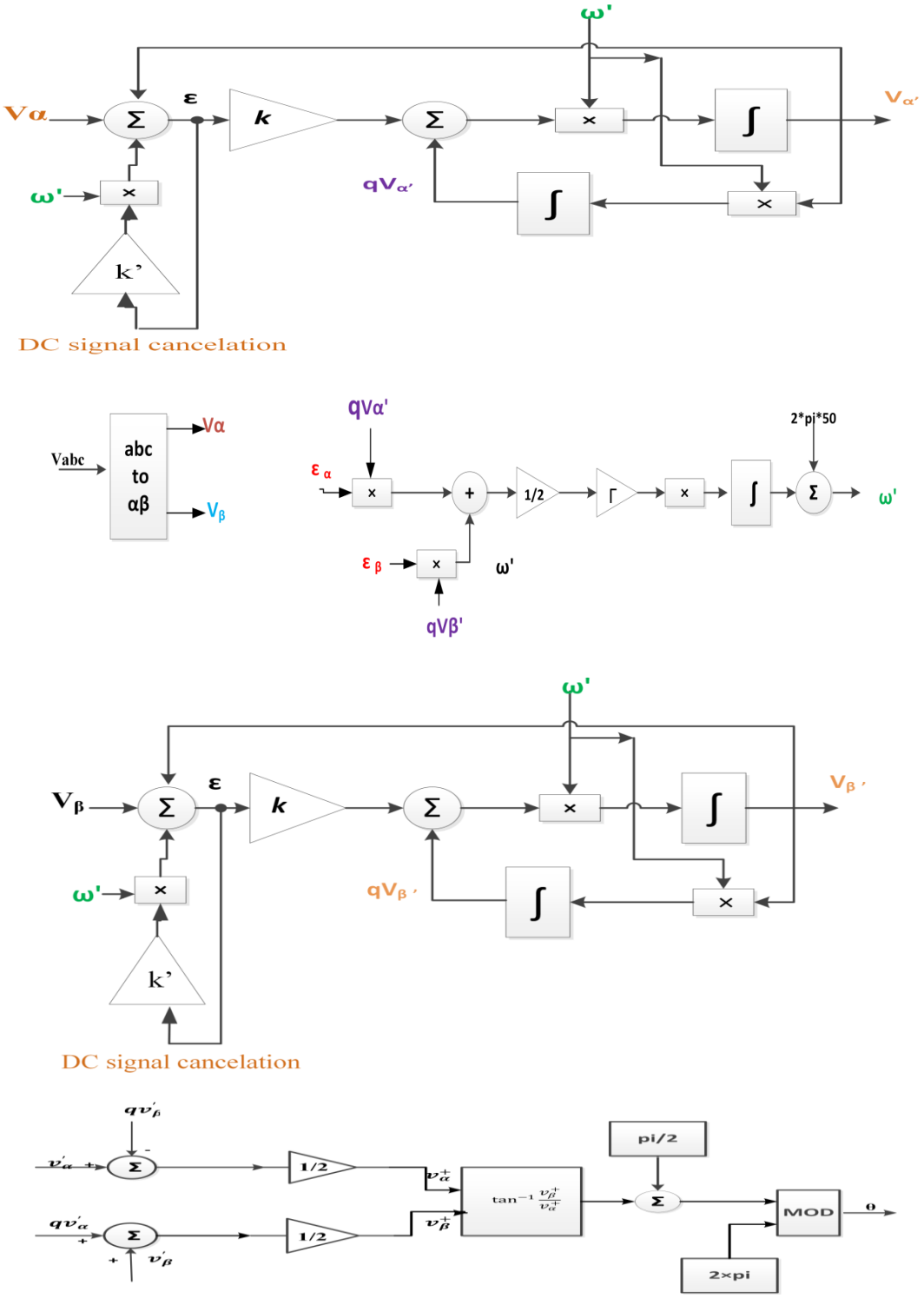


Figure 3-26: Functional diagram of MSOGI-FLLL

When the third integrator determines the DC-offset, it subtracts it from the signal in order to improve the system's DC-offset rejection capabilities, as shown in Figure 3-26 .The proposed

MSOGI-FLL structure, seen in Figure3-26 , includes a DC signal cancellation (DSC) block as well as a SOGI-FLL structure, which is shown in Figure 6. DC-offsets can be injected into the grid signal by signal conditioning or measuring equipment, as well as other factors such as half-wave rectification, which are all common. As a result, the pre-filtering stage has a DC signal cancellation (DSC) block that provides superior DC-offset rejection, as well as a SOGI-FLL block that rejects the low-order harmonic. By integrating the DSC operator in the band-pass DSOGI-FLL (Figure) filter [24], [32], an extended modification of the band-pass SOGI-FLL filter [24], [32] designated as MSOGI-FLL can be presented. For the purposes of comprehension, a grid signal contaminated with a DC-offset and MSOGI transfer functions is represented as follows:

$$D_{MSOGI-FLL}(s) = \frac{Y(s)}{v_{in}(s)} = \frac{k\omega' s^2}{s^3 + k\omega' s^2 + k'\omega' s^2 + \omega'^2 s + k'\omega'^3} \tag{3.73}$$

$$Q_{MSOGI-FLL}(s) = \frac{Y'(s)}{v_{in}(s)} = \frac{k\omega' s}{s^3 + k\omega' s^2 + k'\omega' s^2 + \omega'^2 s + k'\omega'^3} \tag{3.74}$$

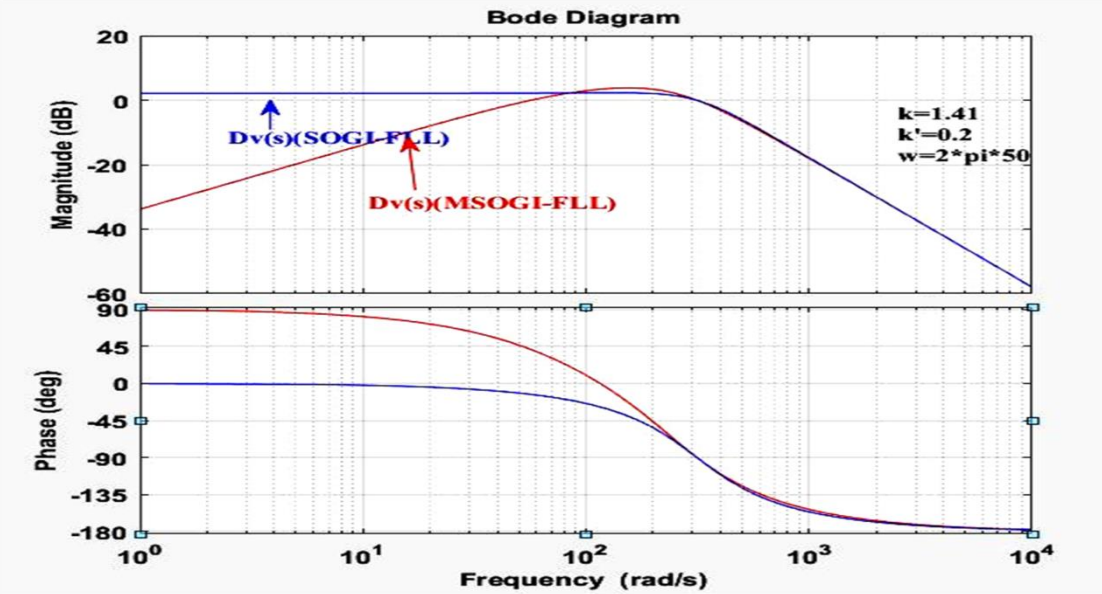
$$E_{MSOGI-FLL}(s) = \frac{V_{dc}(s)}{v_{in}(s)} = \frac{k'\omega' s^2 + k'\omega'^3}{s^3 + k\omega' s^2 + k'\omega' s^2 + \omega'^2 s + k'\omega'^3} \tag{3.75}$$

Using Routh hurtiz criteria, the gain k is given as:

$$k = \frac{9.2}{\omega' t_s};\ t_s = 4.6 * \tau;\ \text{and}\ \tau = \frac{1}{\zeta \omega_n} \tag{3.76}$$

To effectively filter out low and high-frequency components in the input signals, the gain k parameter must be carefully calibrated. Because of this, $D_{SOGI-FLL}(s)$, $Q_{SOGI-FLL}(s)$attenuate low frequency components, leaving just the DC-offset, as depicted in Figure 3-26 and 3-27. MSOGI-FLL transfer functions/characteristic equation MSOGI- FLL($D_{MSOGI-FLL}(s)$, and$Q_{MSOGI-FLL}(s)$) are chosen from the roots of the denominator of the transfer functions/characteristic equation MSOGI-FLL($D_{MSOGI-FLL}(s)$, and$Q_{MSOGI-FLL}(s)$) with equal real parts (Figure 3-27)(all three poles have equal natural frequency of oscillation). To determine the gain k and k', on the other hand, the equation $\omega_{n1} = \omega_{n2}$ =2*pi*50 rad/s (the same as for tuning SOGI-FLL) is employed, which is the same as for tuning SOGI-FLL.The bode graphs in Figure 3-27 demonstrates the impact of both gain adjustments as well as performance assessment of SOGI-FLL and MSOGI-FLL using magnitude plots of transfer functions from equations (3.48)-(3.49) & (3.73)-(3.74), respectively.

(a)



(b)

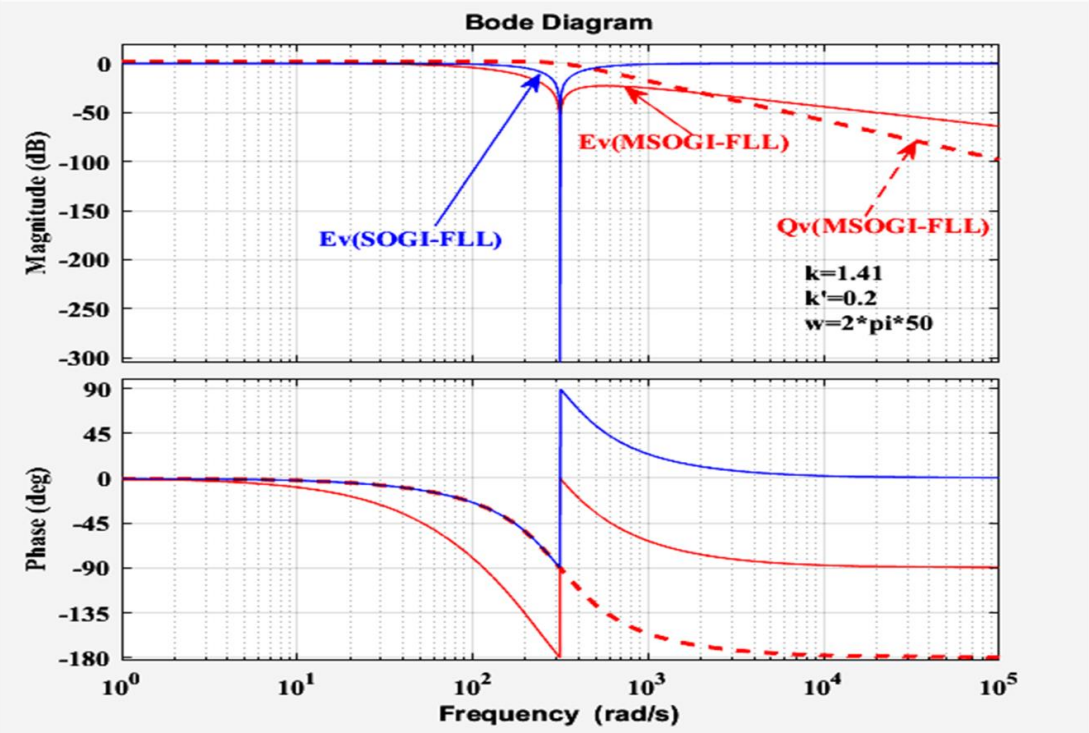


Figure 3-27: Bode diagram of MSOGI-FLL by choosing the value of k and k'.

Figure 3-27(a) and (b) show magnitude bode graphs of $D_{MSOGI-FLL}(s)$and $Q_{MSOGI-FLL}(s)$(equation (3.73)-(3.74)), below 0dB for low frequency components, indicating attenuation of low frequency and dc components. It is clear that a positive gain $Q_{SOGI-FLL}(s)$,which does not reduce the dc signal. Due to presence of third generalised integrator, the magnitude of the transfer function $E_{MSOGI-FLL}(s)$ is close to 0dB. Moreover, $Q_{MSOGI-FLL}(s)$ has negative gain at frequencies over 50Hz, which

reduces higher order harmonics. But it's considerably lower than 50Hz. With the third integrator, the fundamental component (and higher order frequencies) is greatly attenuated, leaving only the low order frequencies to pass, as seen below. It aids in estimating and eliminating the DC-offset from grid voltage. It's feasible to estimate the peak errors in the basic grid's parameters (e.g. amplitude, phase and frequency information), and t_r stands for the settling time performance.

Table 3-3 : Highlights of Comparative Performance Assessment

Cases	Peak Errors	SRF-PLL	SOGI-FLL	MSOGI-FLL
Voltage Drops	ΔA_g	-	-	-
	Δf_g	-	-	-
	$\Delta \theta_g$	-	-	-
	t_r	≈ 80	≈ 55	≈ 45
Freq. Step change (during oveshoot)	ΔA_g	≈ 2	-	-
	Δf_g	≈ 9	≈ 5	≈ 4
	$\Delta \theta_g$	$\approx 5^0$	$\approx 1.5^0$	$\approx 1.5^0$
	t_r	≈ 80	≈ 40	≈ 34
DC-offset Elimination		NO	NO	YES
Harmonics Attenuation		NO	YES	YES
Steady-state Accuracy		Average	Good	Good
Control parameters		2	2	3
PI Tunning Required		YES	NO	NO

The suggested technique takes roughly 2.4 times as long to compute the grid's parameters as the existing standard. With the SOGI-QSG and dc signal cancellation block, MSOGI-FLL can achieve improved immunity to DC-offset and harmonic noise. Both the SOGI–FLL and the SRF-PLL have frequency information that is modified by the phase angle change. However, in the instance of the provided approach, the anticipated frequency has a maximum overrun of 4 Hz. With a net settling time of 34 ms, the recommended single-phase system has demonstrated to have good harmonics reduction and DC-offset rejection characteristics. There is

therefore tremendous potential for the described technology to recognise harmonic and fundamental grid voltage characteristics selectively. Table 3-3 summarizes the experimental findings for the single- phase grid voltage test scenarios.

3.5 Conclusion

The MSOGI-FLL technique can be used to obtain good rejection of DC-offset and harmonics, as well as extraction of frequency and phase-angle information. With the exception of the presence of a DC-offset, SOGI-FLL is capable of accurately estimating the frequency of the grid signal. Because of a DC-offset in grid voltage, the anticipated frequency has a low frequency component of 100Hz due to the DC-offset. When harmonics are present, the distortion on this 100Hz ripple is increased, increasing the overall distortion. As a result of the inaccuracy of the frequency estimate, the synchronization and control of the DG-based inverter may be impaired. In order to achieve the best balance between dynamic responsiveness, filtering capabilities, and the requisite precision in detecting frequency and phase angle for single-phase grid-tied inverters under less than ideal grid conditions, the control parameters of SOGI-FLL must be chosen with care. When the anticipated synchronized frequency is used, there is no ripple in the expected synchronized frequency. This structure is comprised of two fundamental blocks: a standard SOGI-QSG design block that has been updated with a DC-offset cancellation block, and a FLL that is used to compute grid frequency in an adaptive manner. When compared to the regular SOGI-FLL structure, the DC-offset cancellation block (i.e. third integrator) in MSOGI-FLL reduces the DC-offset by a significant amount. Additionally to the advantages of conventional SOGI-FLL, the proposed technique is capable of rejecting DC-offset and, as a result, accurately tracking the fundamental grid-voltage component frequency under all grid abnormalities, hence outperforming the standard technique. The proposed technology is also robust to voltage sags and surges as well as frequency changes in the power grid. The findings of the experiments have revealed that the suggested MSOGI-FLL appears to be more precise and has a higher transient stability than the traditional SOGI-FLL, as demonstrated by the results of the experiments.