CHAPTER-5
EXPERIMENTAL IMPLEMENTATION AND LAB VALIDATION OF SINGLE-STAGE GRID TIED PHOTOVOLTAIC SYSTEM

This chapter presents the experimental lab setup for the multipurpose single-stage grid-tied PV system to carry out test results in different situations. Here, it also demonstrates discrete control system implementation for the multipurpose single-stage grid-tied PV system using WAIJUNG block-set of Simulink/ MATLAB on low-cost digital signal processor base 32-bit ARM core STM32F407VG microcontroller. This chapter describes the design, development, and deployment of a multipurpose grid-tied photovoltaic (PV) system in great depth. Because the inverter is a critical component of a PV system, a laboratory-developed single-stage three-phase inverter is used to reduce the overall cost of a Solar PV system significantly. The suggested multipurpose single-stage grid-tied PV system injects active power into the electric grid and acts as a PV-STATCOM by providing reactive power support to the utility grid. The proposed design is tested on a laboratory-created prototype to see if it works under different test cases.

5.1 Concept of Model based Programming in Simulink/MATLAB using WAIJUNG block-set

It is described in this section the procedures that must be followed during the construction of the model in Simulink/MATLAB for the microcontroller unit. To begin developing a model base program (target Simulink file), open and save a new file in Simulink/MATLAB. The WAIJUNG block-set has many prefabricated blocks that can be used to create a variety of different models. These prefabricated blocks can be turned directly into C code for the specified microcontroller series, whose Simulink/MATLAB third-party supports are available and required. To create any model using the WAIJUNG block-set in Simulink/MATLAB, drag and drop the preconfigured units/ blocks from the WAIJUNG library. Any model design of grid-tied or motor drive application using a voltage source converter must include the following three fundamental blocks:

a) Target setup block: The target setup block defines the compiler, the specific microcontroller IC number, and the base sampling time. This is true for any model built for a particular microcontroller unit. To add this block, open the following place in the library: Click and drag the Target Setup block in WAIJUNG block-set/STM32F4xx Target/Device Configuration. During code generation, the STM32F407VG microcontroller unit is associated with the MDK-ARM compiler, target Simulink file, ST-Link programmer or debugger, and finally, dump code into the microcontroller. Consequently, select the appropriate choice of discrete blocks for the design of control logic from the pull-down menu in the dialogue box in the target Simulink file.

b) Control Logic blocks: In order to construct control logic for any customizable applications, Simulink/MATLAB blocks such as the pulse generator block, sine generator block, and other similar blocks are used in the target Simulink. These blocks establish a model's control logic and generate the necessary control signals/firing pulses for any application.

c) Input/output blocks: To transfer the generated control signals to the appropriate GPIOs for further transmission, the predefined Input/ Output blocks included in the WAIJUNG block-set are used. To add this/these blocks, the following library location must be opened: Click and drag the required block/s from the WAIJUNG block-set/STM32F4xx Target/On-chip peripherals. The DAC and ADC can be used to create a closed-loop control system. Additionally, the WAIJUNG block-set includes a pulse width modulation (PWM) block, an advanced PWM block (inherent dead band of 1 micro-second between complementary pulses), and a timer block for constructing sophisticated models. Using the model configuration parameter, the discrete model solver should be selected in Simulink/MATLAB. The model is now ready to be dumped into the STM32F407VG ARM cortex microcontroller, which can be done by clicking on the build command icon in the Simulink file. The build command can be issued in three ways: 1) Select the code menu. C/C++ source code 2) Select the Build model option, or 3) press control + B. The code generation process has gone through the following procedure: produce

source code, pack source code, compile source code, connect to target, Erase the entire chip, download and verify, and run the target. These procedures are carried out automatically when the build command is used. After completing these processes, the target file hex code is dumped into the microcontroller. This concludes the process of generating gate signals. These gate signals are gathered on the GPIO pins and routed via jumpers to the power card.

5.1.1 Overview of ARM Cortex M4 STM32F4 microcontroller

This section describes a customizable and cost-effective experimental development for the grid-tied system in context to the microcontroller. Additionally, the controller selected determines the complexity of generating gate signals. For traditional DSPs and microcontrollers like the 8051, there must be well-versed in writing code in order to generate gate signals. Alternatively, the gate signals can be generated using an ARM Cortex M4 microcontroller, WAIJUNG block-set, and Keil. Using the Simulink/MATLAB models, the WAIJUNG block-set used target Simulink file is automatically translated to C and then dumped into the microcontroller memory. Simulink/MATLAB WAIJUNG block-set blocks can be directly used to generate the signals, eliminating the need for coding [11]. [10, 11] This study emphasizes low-cost hardware design. For a single piece of hardware setup (STM32F407VG, IGBT-based power card, current and voltage sensors, and three-phase driver card included), the cost is relatively low. Additionally, the same hardware configuration may be utilized to build a variety of other experiments or carry out different test cases of the grid-tied PV system. Arm Cortex M4 32-bit microcontroller from STMicroelectronics STM32F407xx is designed for high-efficiency digital processing and has a wide range of peripherals. 210 million instructions per second (MIPS) may be processed, and a single cycle multiplication and accumulation can be performed. This microcontroller has several valuable features, including 1) A LQFP100 package with 1MB of Flash memory and 192KB of RAM operates at a maximum frequency of 168 MHz, resulting in a maximum throughput of 210 MIPs. St-LINK/V2 hardware debugger onboard for in-depth hardware troubleshooting (SWD connector for programming and debugging); the A/D converters are 3x12-bit, 2.4 million samples per second, while the D/A converters are 2x12-bit, 2.4 million samples per

second. Direct memory access (DMA) controller with FIFOs and burst support for 16 streams, general-purpose twelve 16-bit and two 32-bit timers up to 168MHz, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder inputs, and up to 17 totals. A total of six additional PWM channels with adjustable dead time insertion are available. More than a dozen different communication interfaces, such as UART and SPI. A maximum of 140 GPIOs (general purpose input and output) are supported, as well as ten 5V-tolerant GPIO pins, Floating-point unit [11], and Incremental Encoder interface [12] are included in this section. ARM Cortex 32-bit M4 microcontroller is used as the controller board since it is less expensive and easier to program.

5.2 Experimental Modeling of Multipurpose Single-Stage PV System in MATLAB/Simulink

The multipurpose single-stage PV inverter controller model is designed in Simulink/MATLAB software and implemented on the 32-bit ARM cortex microcontroller. In the Simulink target model, sensed three-phase inverter current, load currents, and voltage signals are assigned to specific analog-to-digital (ADC) channels. In other words, DC-bus voltage, the inverter current, load current, and PCC voltage are read by ADC channels from sensor cards. The controller design is built on the mathematical model described in chapter 4. The simplified multipurpose single-stage PV inverter controller in Simulink are explained in comprehensive

5.2.1 Discrete control system in synchronous reference frame for Single-stage grid tied PV system using WAIJUNG code

The Discrete control system of a grid-tied PV system is modeled and realized in Simulink/MATLAB environment using WAIJUNG block-set, as depicted in Figure 5-1. The target Simulink STM32F4 model presented in Figure5-1 is configured to read DC-bus voltage, three-phase voltages, three-phase load currents, and three-phase inverter currents.

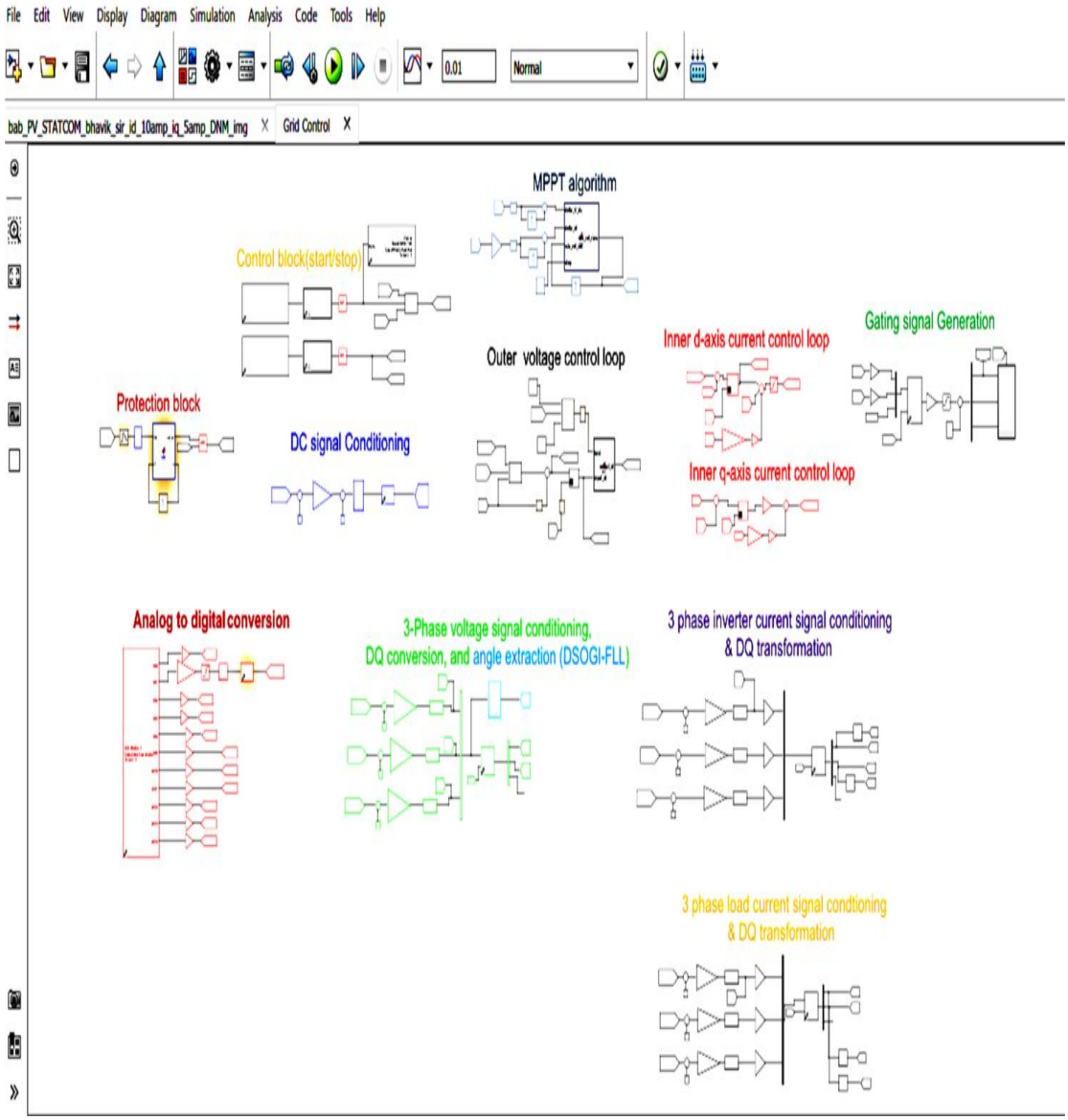


Figure 5-1: Target Simulink/MATLAB diagram for the control system of Multipurpose Single-stage grid tied PV System

The target Simulink STM32F4 model of a discrete control system for grid-tied PV system is realized by the following key blocks: (1) Analog to digital conversion block to read DC-link voltage, three-phase voltages, three-phase inverter currents, and three-phase currents, (2) DC signal conditioning, (3)Transformation phase voltages, inverter currents, and load currents from three-phase system to synchronous frame,(4) Grid voltage phase-angle extraction for grid synchronization,(5) DC-link voltage reference computation from MPPT, (6) The outer voltage control loop,

(7)D-axis inner current control loop, (8) Q-axis inner current control loop, (9) PWM signals generation, (10) ON/OFF control block, and (11) Protection Block. Furthermore, a difference of d-axis current reference and actual d-axis current component as input of PI regulator decides the amount of active current injected to the utility grid by generating PWM signals using space vector modulation technique.

5.2.2 Design or Implementation of a signal conditioning circuit

In a signal conditioning circuit, current and voltage transducers are used in simultaneously. In the present work, a DC voltage transducer is hall effect based sensor, whereas AC voltage sensors and AC current sensors circuit are designed using potential transformer, which were used to sense and transform high power quantities as, such as three-phase currents and voltages, into low-level analogue voltage signals in the range of +3V DC or 0V to 3V AC signal by DC voltage sensor and AC voltage and current sensors respectively. The Hall Effect voltage sensor provides galvanic isolation between the primary circuits (which are high power) and secondary circuits. Figure 5-2 shows a schematic block diagram of the Hall Effect voltage transducer along with op-amp based amplifier with amplification gain(A_{gain}).In laboratory prototype, voltages have been reduced from 250V to 3V for the ADC pin of microcontroller. The sensed output is retrieved from the measurement at output of hall sensor, which is actually output of amplifier. The voltage transducer, for example, requires a supply voltage of 15 V and can measure both AC and DC voltages in the range of 10–500 V. Notably, the input resistance R_{in} (Potentiometer,$100K\Omega$) should be chosen so that the output measurement resistance R_{out} (Potentiometer,$1K\Omega$) falls within the range of 100–300 as described in the datasheet for hall base voltage transducer. For a DC-link voltage 250 volt and R_{in} is set to value $100K\Omega$, I_{in} is computed as follows:

$$I_{in}=\frac{V_{dc_{sensed}}}{R_{in}} = \frac{250}{50\times10^{3}} = 5mA \quad (5.1)$$

Furthermore, the amplification gain of op-amp base amplifier is gain ($A_{gain} = 3$).

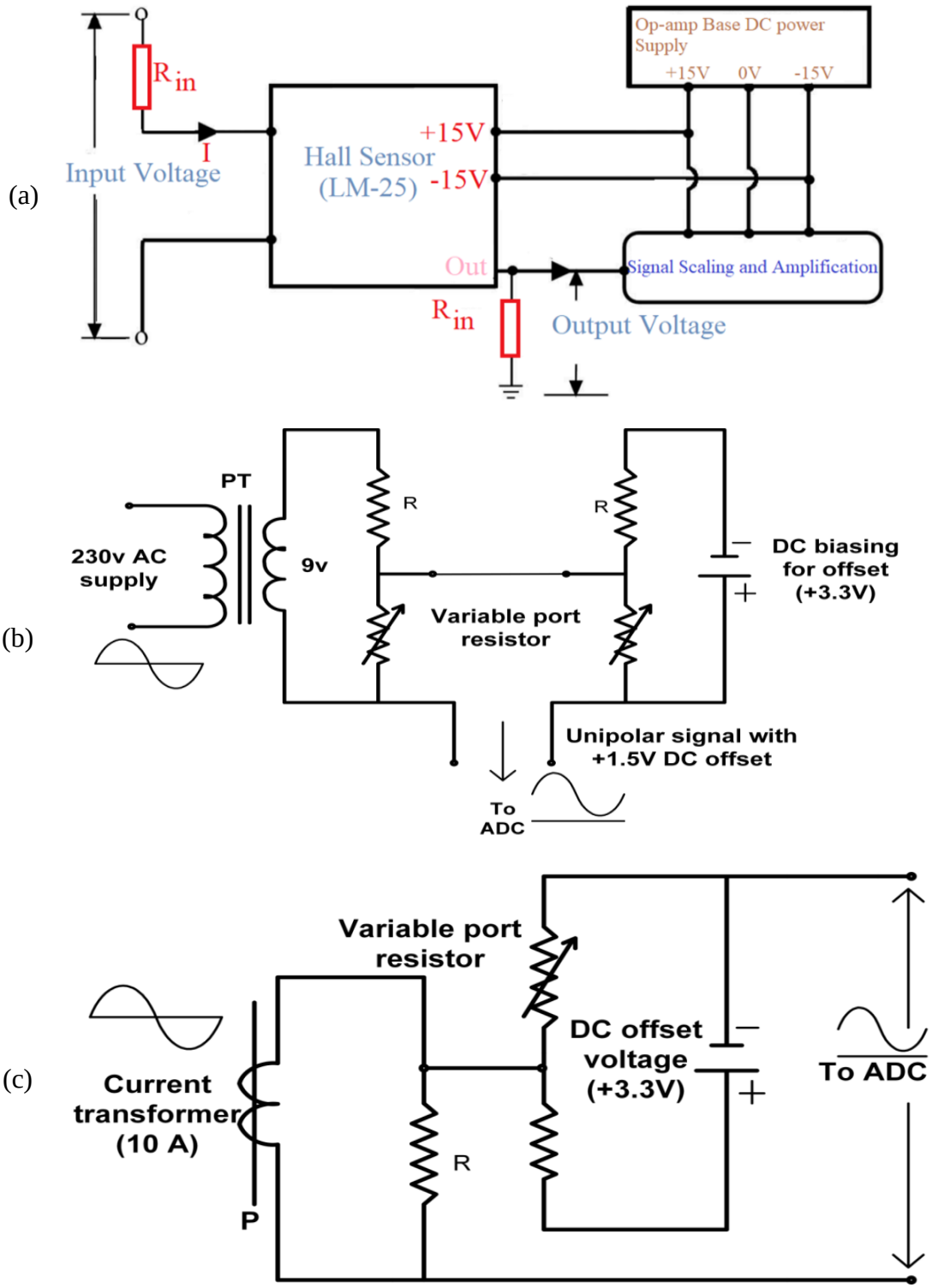


Figure 5-2: Schematic Diagram of (a) voltage Hall sensor circuit, (b) AC voltage sensor circuit using Potential divider and voltage transformer, and(c) current transformer circuit with DC-bias

Consequently, I_{out} is calculated as follows:

$$I_{out} = A_{gain} \times I_{in} = 3 \times 5mA = 15mA \quad (5.2)$$

Assumptions are obtained for the output measurement resistance R_{out} (Potentiometer, 1KΩ) to obtain 3 V when the 250 V input is applied. The output measurement resistance R_{out} is computed as:

$$R_{out} = \frac{V_{output}}{I_{out}} = \frac{3V}{15mA} = 200\Omega \quad (5.3)$$

The output measurement resistance R_{out} is set around 200Ω in a potentiometer. The three-phase voltages are sensed with the help of three Potential Transformers (PTs). Figure5-2(b) shows the schematic of the AC voltage sensing arrangement in which three single-phase potential transformers of rating 230/9 volts are used. Since all the phases are identical, only a single phase arrangement is shown in Figure 5-2. The voltage divider method is used to reduce the AC voltage output from those potential transformers. DC offset is required in this case to convert sensed voltages into positive values (unipolar signal); this has to be done because the input of ADC of the microcontroller must be positive (or unipolar). The value required for this DC offset is itself taken from the microcontroller. Similarly, the voltage divider method is used in the DC offset circuit. The three-phase currents are sensed with the help of three Current Transformers (CTs). Figure 5-2(c) shows the schematic of the AC current sensing arrangement in which three single-phase current transformers of rating 10A/500mA are used. Burden resistors are connected across CTs. As all three phases are identical, only a single-phase arrangement is shown in Figure 5-2. The voltage divider method is used to reduce the voltage output across the burden resistor. Similarly, as in the AC voltage sensing circuit, the voltage divider method in the DC offset circuit is used to convert sensed voltages into positive values; this has to be done because the input of the ADC of the microcontroller must be positive.

5.2.2.1 Brief description of Analog to Digital PINs in WAIJUNG Block-set

The Analog-to-Digital Converter (ADC) converts analog voltage/ current signal into a digital signal. The STM32F407VG microcontroller has three 12-bit ADCs. The ADC offers sample rates of 2.4 million per second and 12-bit resolution. It is feasible

to sample all three ADCs simultaneously on the ARM cortex STM32F407 microcontroller 24 channels. Control blocks can be built using the ADC and DAC for closed-loop applications. In Figure 5.3, the regular ADC units read the voltage/ current of configured pins and produce a value ranging from 0 to 4095 based on the reading. There is no voltage at the input side of the ADC pins, as indicated by the output ADC value of 'Zero'. However, the output ADC value of 4095 implies that there is 3 volts at the input side. Thus, if the output is multiplied by the gain 3/4095, then should get actual value of analog voltage inside the code for the control system. As previously indicated, the Discovery board requires a voltage supply between 0 and +3 volts. Voltages that are either too positive (more than +3.3 V) or negative voltage can damage the board.

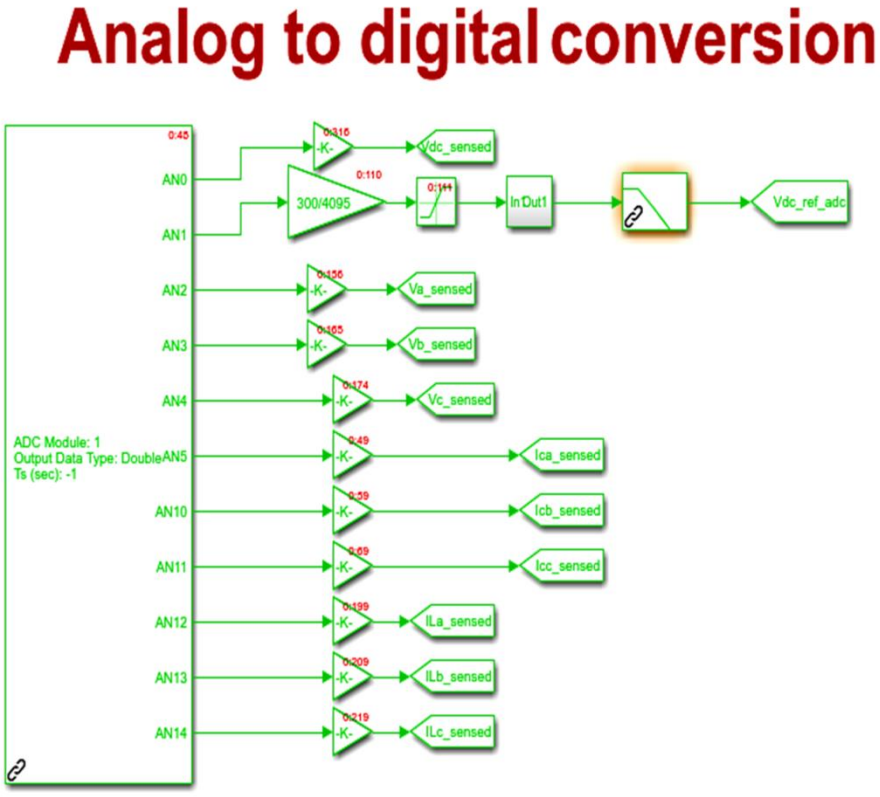


Figure 5-3: Configuration view of A/D converter in the target Simulink

The Pins AN0, AN1 are configured for sensed DC-bus voltage and reference value of DC-bus (instead of MPPT algorithm), which can be varied by the 0V to 3V potentiometer. The ADC pins AN2,AN3and AN5 are configured for three phase inverter currents, whereas load current are configured on ADC pins AN12,

AN13,AN14.As depicted in Figure 5-4, the pre-scaler value is chosen to 2.

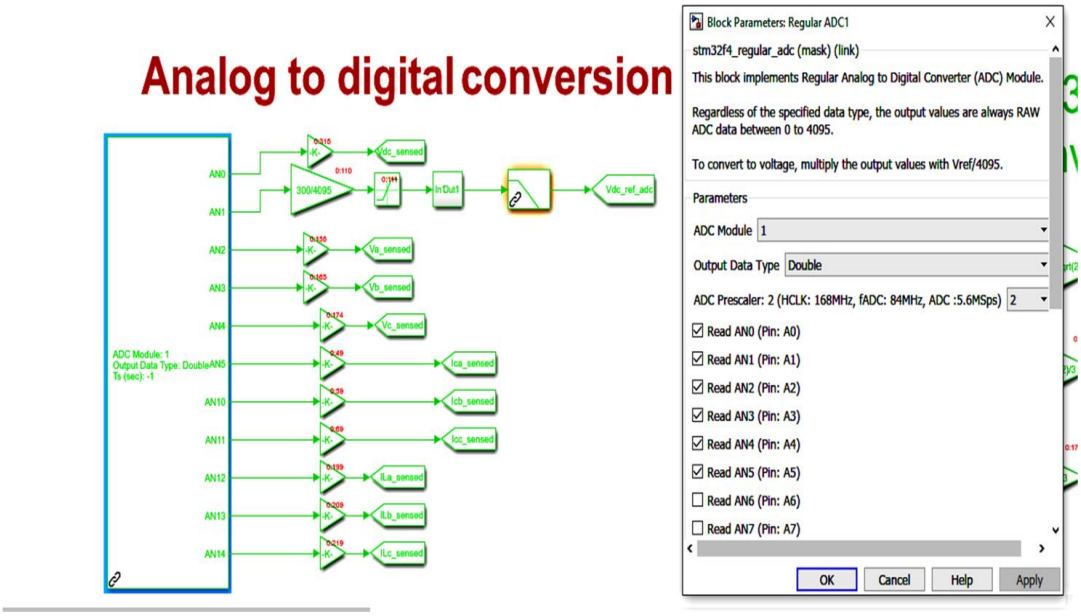


Figure 5-4: Configuration view and Pin assignment of A/D converter in the target Simulink

The reference value of DC-bus can be varied from 200V to 300V at the ADC pin AN1 by multiplying the gain$\frac{300}{4095}$ and saturation block make sure the variation in the range of 200V to 300V. The sensed three phase inverter currents and sensed three phase load currents are multiplied by gain $\frac{3}{4095}$ value inside code, as depicted in Figure 5-4.

5.2.2.2 Description of Control block (start/stop) in WAIJUNG block-set

The control block plays a crucial role in controlling the grid-tied PV system. Here, two common ground push switches are connected to the PD7 for the ‘ON’ or ‘OFF’ either start or stop gating pulses from the microcontroller as well as reset the PI controller, and PD5 for the shifting from fixed DC-bus reference voltage (250V) to varying DC-bus reference voltage from 200V to 300V through the external potentiometer. The pin PD15 of the microcontroller is interfaced with a common anode base LED, which is used as a status indication of PD5. If PD5 is ‘1’, then fix DC-bus reference voltage (250V) is given to the outer loop voltage control of grid-tied PV system, whereas PD5 is ‘0’, then variable DC-bus reference voltage from

200V to 300V through the potentiometer is given to the outer loop voltage control of grid-tied PV system. Here, PD5 and PD7 are configured as input switches and used in Toggle mode for the stop/ start of the control system.

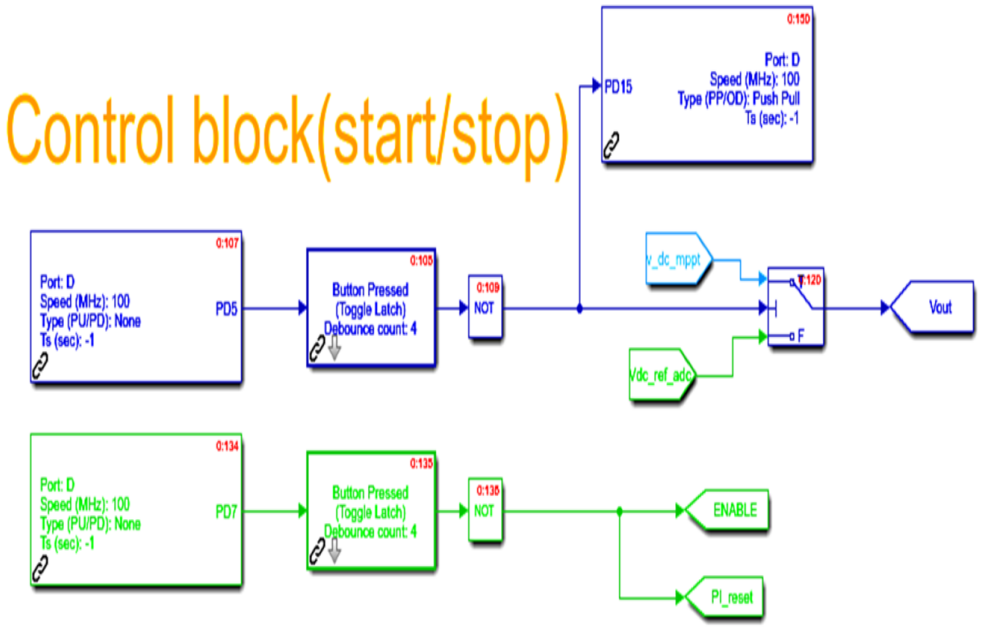


Figure 5-5: Configuration schematic of Start/Stop of gating pulses control in the target Simulink

5.2.2.3 Description of DC-bus voltage signal conditioning in WAIJUNG block-set

An actual DC-bus voltage is sensed, which is scaled from 250 volt to 3volt using hall sensor and signal conditioning circuit, and fed to ADC pin of microcontroller. Inside the model base program code, sensed DC-bus voltage is converted into actual value of DC-bus voltage by multiplying gain of $\frac{250V}{3V}$ and fed to discrete moving average filter to obtain ripple free actual DC-bus voltage, as depicted in Figure 5-6.

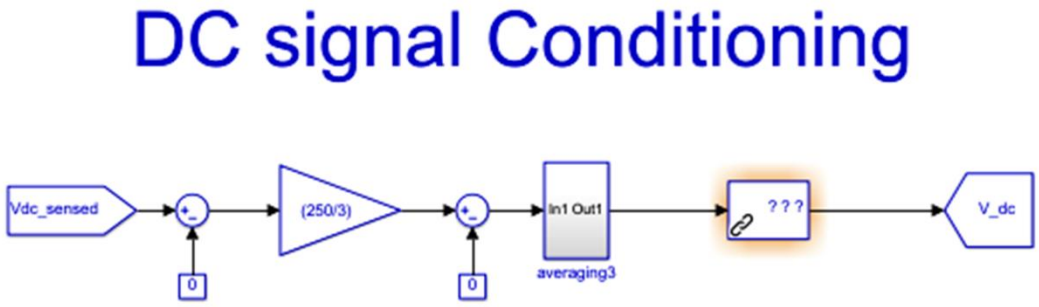
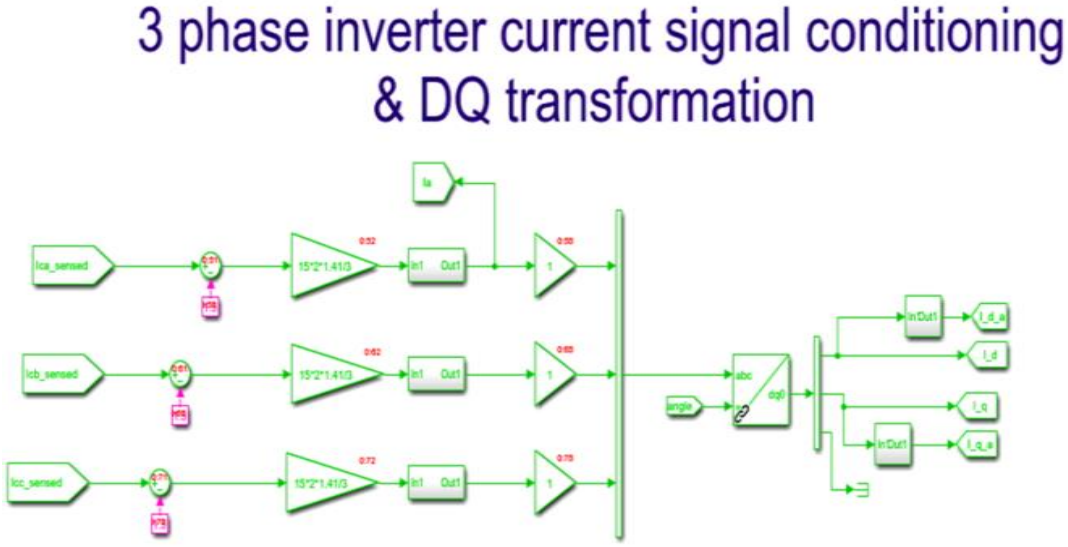


Figure 5-6: Configuration schematic of DC signal conditioning in the target Simulink

5.2.2.4 Description of synchronous reference frame transformation in WAIJUNG block-set

Synchronous frame power control can be implemented using a current controller in a dq frame (Figure 5-7) and active and reactive power feed-forward control in the simplest way possible. The reference voltage for the active power can be altered by controlling the DC voltage. A matrix is used to convert the command signals into the dq components of the reference current.

(a)



(b)

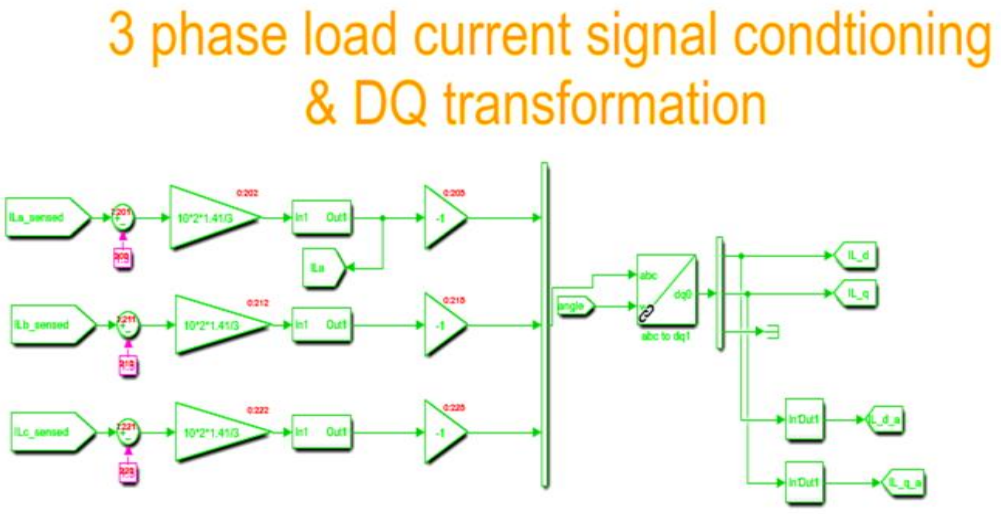


Figure5. 7: Configuration schematic of DQ transformation for (a) three-phase inverter currents, and (b) three phase load currents in the target Simulink

Signal conditioning circuits is employed to add DC offset of 1.5V in sensed inverter and load currents to generate uni-polar signals for the ADC pins. In side code, 1.5 V DC-offset eliminated first, then multiplied by the gain value $\frac{1.5\times2\times1.41}{3}$ to obtain actual inverter currents and load currents. Eventually, the abc three-phase stationary frame is transformed into synchronous reference frames dq0.The synchronous reference frames dq0 component of inverter currents as well as load currents are defined by a transformation matrix derived from the abc three-phase stationary frame using phase-angle of utility grid voltages (θ_{v_g}) and computed as:

$$\left[i_{dqo}\right] = \sqrt{\frac{2}{3}} \times \begin{bmatrix} \cos(\theta_{v_g}) & \cos(\theta_{v_g} - \frac{2\pi}{3}) & \cos(\theta_{v_g} + \frac{2\pi}{3}) \\ -\sin(\theta_{v_g}) & -\sin(\theta_{v_g} - \frac{2\pi}{3}) & -\sin(\theta_{v_g} + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \end{bmatrix} \quad (5.4)$$

The currents, i_{dqo} , are fed to discrete moving average filter to eliminate ripple from DC quantities. The ripple free d-axis and q-axis component of inverter currents and load currents are obtain from the sub system as shown in Figure 5-7(a) and 5-7(b).

5.2.2.5 Grid Synchronization in WAIJUNG block-set

The phase-locked loop (PLL) is used in grid-tied systems to synchronize converter operation with the grid voltage. The bandwidth of an irregular grid should be decreased to enable appropriate disturbance rejection without compromising detection speed. PLLs must increase dynamic response and minimize settling time without compromising system stability or the ability to eliminate disturbances. Control approaches with SOGI-FLL (second-order generalized integrator-frequency locked loop) performed the best for a single-phase /three phase system. It tracks harmonics, voltage changes, and frequency fluctuations precisely. This means that the SOGI-PLL outperforms the other PLLs in terms of speed and accuracy in poor grid circumstances, and detailed analysis is presented in chapter 3. A dual SOGI-FLL (DSOGI-FLL) structure is employed to extract positive component of grid voltages (v_{α}^{+} and v_{β}^{+}) during the abnormal grid (harmonics distortions, voltage imbalances, frequency changes, voltage imbalances, etc.), which is formed by two SOGI blocks connected in parallel as depicted in Figure 5-8. .

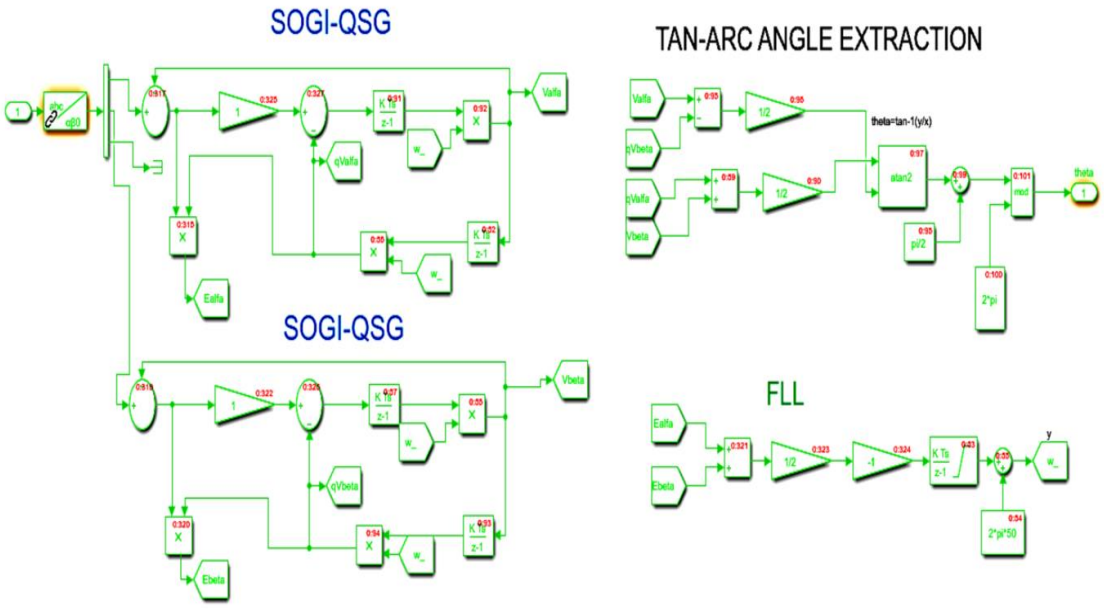


Figure 5-8: Configuration schematic of modified SOGI-FLL and angle computation block in the target Simulink

The positive component of grid voltages (v_α^+ and v_β^+) are fed to the phase-angle extraction unit, which is formulated based on tan-arc angle extraction method, as depicted in Figure5-8. The Frequency Lock loop is formulated for the frequency extraction.

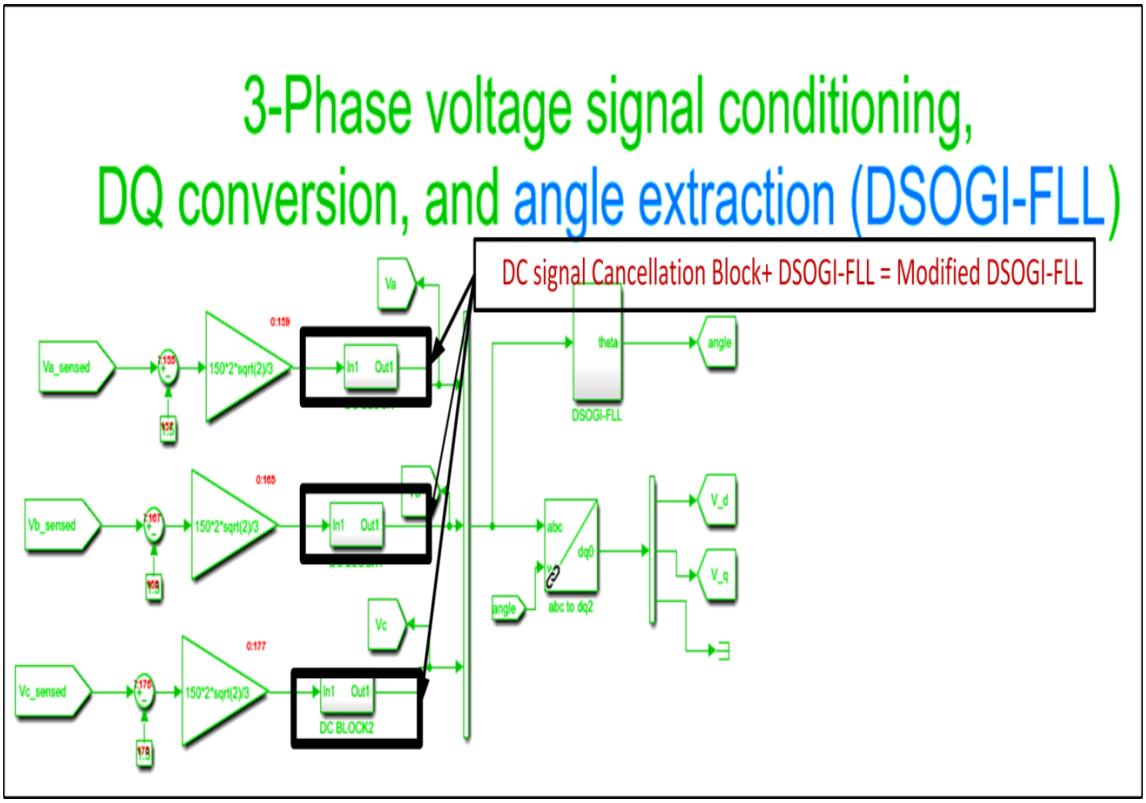


Figure 5-9: Configuration schematic of DQ transformation for the three phase voltage signal in the target Simulink

Figure 5-9 shows three-phase grid voltages and DSOGI-FLL phase angle. The effectiveness of DSOGI-FLL is tested by taking different situations like frequency change, phase change, unbalancing of three-phase voltages, harmonics distortion, and DC offset. The target Simulink model for test cases is modeled and shown in Figure 5-10. The internal three-phase grid voltages are designed using components from the Simulink library, as depicted in Figure 5-10. The amplitude, phase, and frequency internal three-phase grid voltages can be controlled, changed or varied using three potentiometer 3V at ADC pins or an internal conditional switch with two constant values controlled by an external push switch.

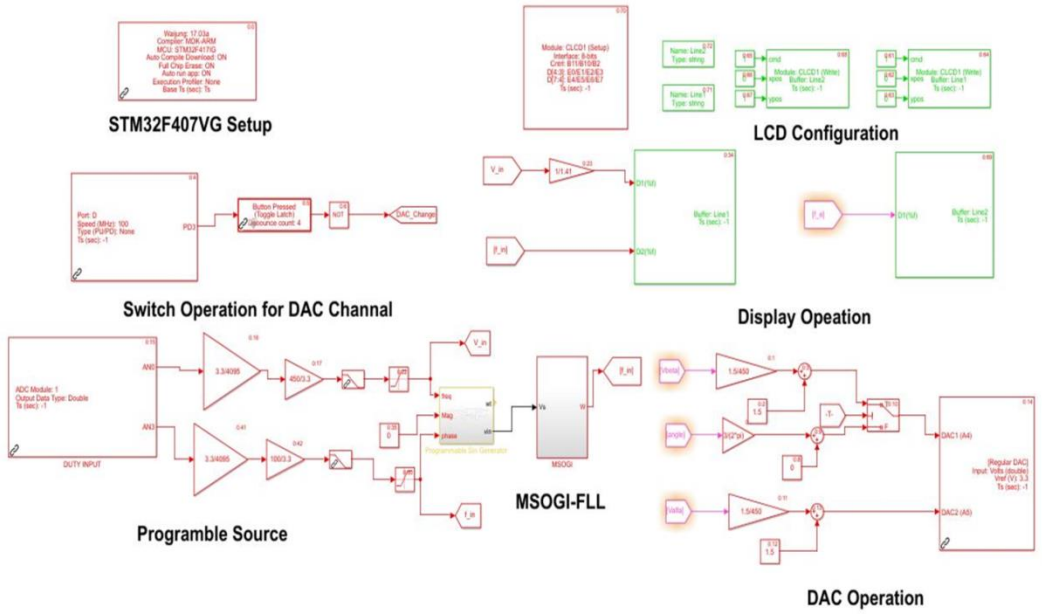


Figure 5-10: Test bench schematic diagram for Modified SOGI-FLL by designing programmable source in the target Simulink

The frequency and phase sift are applied simultaneously, so, the variation of frequency can be observed in digital oscilloscope. For the frequency shift of 10% (frequency change from 50Hz to 45Hz) and phase-shift of 45°in three phase grid voltages, the conditional switch gives 50Hz value and phase of 0° to the frequency input and phase–angle of internal three-phase grid voltages when the status of external switch is '0' , while 45Hz value and phase of 45° to the frequency input and phase –angle of internal three-phase grid voltages when the status of external switch is '1', as depicted in Figure 5-11. The ARM cortex STM32F407VG has two Digital/ analog converter peripherals to observer signal, but, amplitude must be less than 3V. Figure 5-11(a) displays three-phase grid voltages along with the phase-angle extracted by DSOGI-FLL. The three-phase grid voltages, displayed in Figure 5-11(a), undergoes a frequency shift of 10% (frequency change from 50Hz to 45Hz) and phase-shift of 45° to observe the frequency change. The frequency and phase shift in the three-phase grid voltages are measured by taking difference of cursor positions before and after frequency and phase shift, shown in the Figure 5-11(b). The estimated frequency is settled down to the new frequency of 45 Hz within 35 mille-seconds, as shown in the Figure.5-11 (c) and (d). Figure 5.11

shows the three-phase grid voltages along with extracted phase-angle from DSOGI-FLL

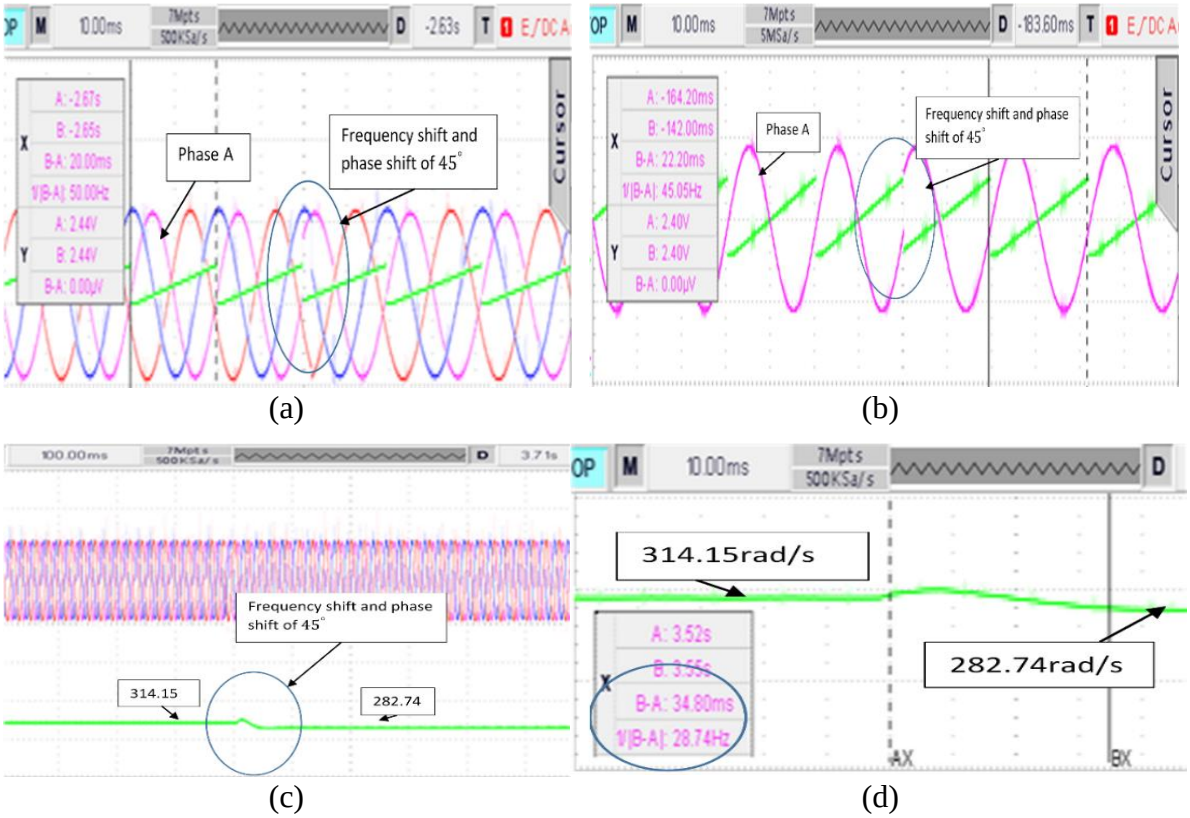
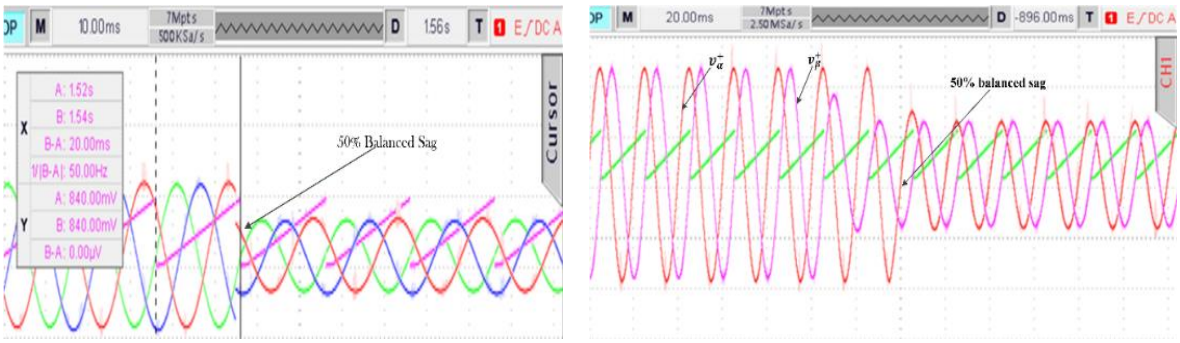


Figure 5-11:Experimental results obtained from test bench of SOGI-FLL and measured during 10% frequency and 45° phase shift in grid voltages: (a) three-phase voltage signals and phase –angle of grid, (b)Zoom view of phase-a voltage signal of three phase and phase(c) dynamic performance of angular frequency, (b)Zoom view of dynamic performance of angular frequency

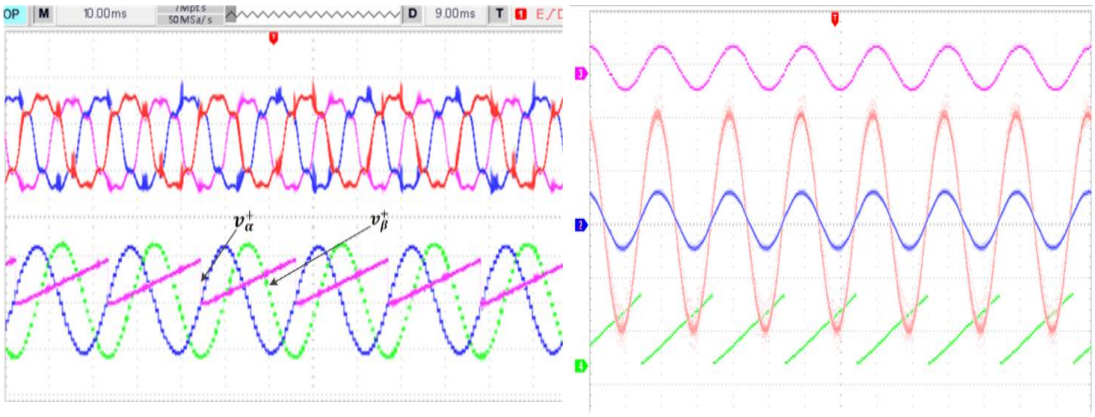
It is noted that extracted phase-angle from DSOGI-FLL is not affected much more when initially balanced grid voltage experiences the balanced sag of 50%, as shown in the Figure 5-12. Figure 5-12 (b) shows the positive sequence of grid voltages i.e.v_{α}^{+} and v_{β}^{+} and along with extracted phase-angel from DSOGI-FLL. During the voltage sag, frequency and extracted phase-angle is settled down within two cycles i.e. around 35 milli-second, as shown in the Figure 5-12. The DSOGI-FLL behaves as second-order band-pass filter, which provides immunity towards highly distorted three-phase grid voltages.



(a) (b)

Figure 5. 12:Experimental results obtained from test bench of SOGI-FLL during 50% balanced sag in the grid voltages

The three-phase grid voltages experience the presence of 5th, 7th,11th order harmonics with amplitude proportional 20%, 15%,and 10% respectively, as shown in the Figure 5-13. It is noted that DSOGI-FLL is capable to eliminate the negative sequences and harmonics component from grid voltages. Figure 5-13 shows the highly distorted grid voltages, the positive sequence of grid voltages i.e.v_{α}^{+} and v_{β}^{+} and along with extracted phase-angel from DSOGI-FLL. The DSOGI-FLL gives superior performance when grid voltages experience multiple abnormalities at the same time. It is also observed that extracted phase-angle is free from high frequency components due to the distorted grid voltages. In the event of a DC offset, the calculated frequency incorporates low frequency oscillations. A modified second-order generalized integrator frequency-locked loop (MSOGI-FLL) is presented in this work to address grid voltage anomalies of all types, including dc offset. Figure 5-13(a) shows the positive sequence of grid voltages i.e., v_{α}^{+} and v_{β}^{+} and along with extracted phase-angel using DSOGI-FLL from distorted grid voltages with 10% DC offset. Figure 5-13(b) shows the result of single-phase grid connected system. As described in previous section, ADC pin accept only unipolar signal. So, AC signal is converted to unipolar signal by adding 1.5Volt DC offset while inside code same amount(1.5Volt) is subtracted from signal at ADC pins to obtain actual signal. The DC offset is added by improper elimination of DC scale. Instead of 1.5 Volt, 1.3Volt is subtracted from signal which is at ADC pins to get actual signal. In this way, grid voltage is encounter by DC offset.



(a) (b)

Figure 5-13:(a) Experimental results for grid synchronization during grid voltages effected by the harmonics, and (b) Experimental results of single-phase grid interfaced voltage source converter (Time scale:10ms//div) : i_g (Pink and blue; Scale 2A/div), v_g (Orange; Scale: 40V/div), and theta(green)

It is noted that modified DSOGI –FLL eliminates both harmonics distortion and negative sequences of three-phase grid voltage in order to detect accurately phase-angle of the grid voltage during abnormal grid voltage conditions including DC offset.

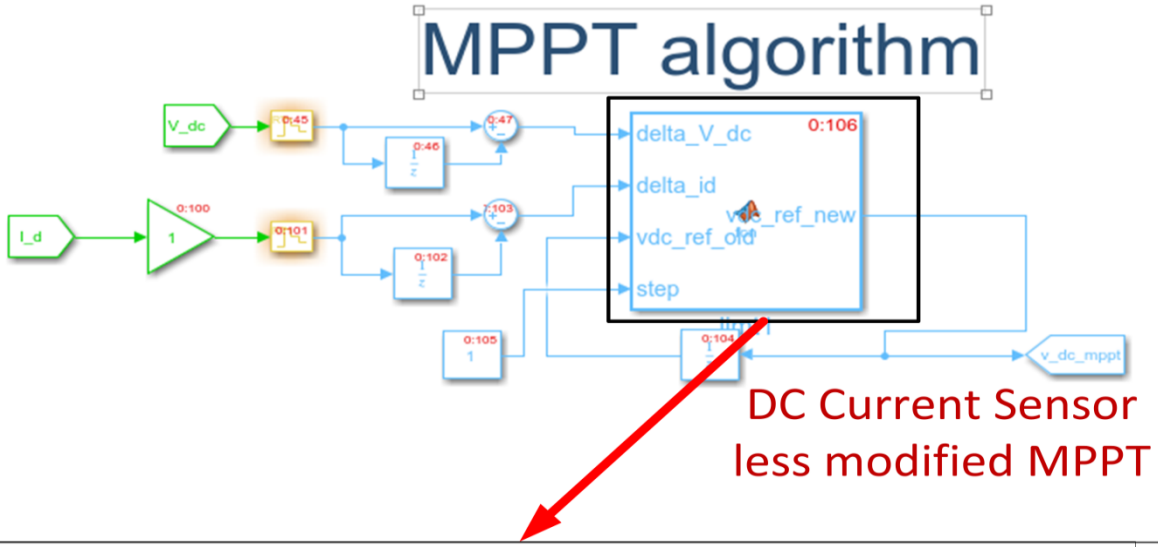
5.2.2.6 DC Current sensor less modified MPPT algorithm in WAIJUNG block-set

Figure 5-14 shows DC current sensor less modified MPPT algorithm for Single-stage grid tied PV system. The modified MPPT algorithm code is written in user define function of Simulink. The target Simulink file is modelled using multi-processing sampling rate. Here, modified MPPT algorithm (user define function of Simulink) is sampled at time interval which is 100 times of sampling time of target Simulink, as depicted in blue color. It is possible to estimate the reference value of d-axis current component by utilizing the DC-bus voltage regulator. It is necessary to compare the reference DC-bus voltage ($V_{dc_{ref}}$) produced from the MPPT scheme with the actual DC-bus voltage (V_{dc}) in order to determine the voltage error (ε_{dc}), which is minimized by employing a PI regulator.

$$\varepsilon_{dc}[n] = (V_{dc_{ref}}[n] - V_{dc}[n-1] \quad (5.5)$$

$$I_{d_{ref}}[n] = I_{d_{ref}}[n-1] + K_{P_{dc}}.(\varepsilon_{dc}[n] - \varepsilon_{dc}[n-1]) + K_{integral_{dc}} T_{s_{dc}}.\varepsilon_{dc}[n] \quad (5.6)$$

Here, $K_{P_{dc}}$ and $K_{integral_{dc}}$ are the proportional and integral gains in voltage controller, respectively. In the outer DC-bus control loop, $T_{s_{dc}}$ is a sampling time for outer voltage control loop. A Photovoltaic inverter provides reactive power up to the inverter's maximum VA capacity. A reference value of q-axis component for the PV inverter current, $I_{q_{ref}}$, which is chosen based on the operating mode of the inverter. The power factor at PCC is controlled by $I_{q_{ref}}$, which is derived by multiplying the negative unity gain to the q-axis component of the Load current, $I_{q_{Load}}$ in Mode I.




```
function vdc_ref_new = fcn(delta_V_dc,delta_id,vdc_ref_old,step)
      if (delta_V_dc>0)
           if (delta_id>0)
            vdc_ref_new=  vdc_ref_old + step;
           else
            vdc_ref_new=  vdc_ref_old - step;
           end
      else
           if (delta_id>0)
           vdc_ref_new=  vdc_ref_old - step;
           else
           vdc_ref_new=  vdc_ref_old + step;
           end
      end
      if(vdc_ref_new<180)
           vdc_ref_new=180;
      elseif (vdc_ref_new>240)
            vdc_ref_new=240;
      else
           vdc_ref_new=vdc_ref_new;
      end
    end
```

Figure 5-14: Configuration View and m-file of modified MPPT algorithm

In Mode I (power factor control), $I_{q_{ref}}$ is expressed as follows:

$$I_{q_{ref}}[n] = -1 \times I_{q_{Load}}[n] \quad (5.7)$$

Mode II $I_{q_{ref}}$ is derivable from the PI regulator, which is employed to manage grid voltage at PCC and is hence derivable from the PI regulator. It can be deduced from Mode II (grid voltage control) as follows:

$$\varepsilon_{PCC}[n] = (V_{peak_{ref}}[n] - V_d[n-1]) \quad (5.8)$$

$$I_{q_{ref}}[n] = I_{q_{ref}}[n-1] + K_{P_{PCC}}(\varepsilon_{PCC}[n] - \varepsilon_{PCC}[n-1]) + K_{integral_{PCC}} T_{s_{PCC}} \varepsilon_{PCC}[n]) \quad (5.9)$$

Here, $K_{P_{PCC}}$ and $K_{integral_{PCC}}$ are the proportional and integral gains of the PCC voltage regulator. In the outer PCC voltage control loop, $T_{s_{PCC}}$ represents the sampling time. It is possible to calculate the PCC voltage error (ε_{PCC}) by subtracting the measured peak value of PCC voltage V_d from a peak reference value of PCC voltage$V_{peak_{ref}}$.

5.2.2.7 Synchronous Frame current control in WAIJUNG block-set

Equation (5.10) to (5.12), which contain the values of $I_{d_{ref}}[n]$ and $I_{q_{ref}}[n]$, are used to control $I_d[n]$ and $I_q[n]$ with the use of two current regulators.

It is possible to realize these two current regulators using the following equations:

$$\varepsilon_{i\_d}[n] = (I_{d_{ref}}[n] - I_d[n-1]) \; ; \; \varepsilon_{i\_q}[n] = (I_{q_{ref}}[n] - I_q[n-1]) \quad (5.10)$$

$$V^*_{d_m}[n] = V^*_{d_m}[n-1] + K_{p_{i\_d}}(\varepsilon_{i\_d}[n] - \varepsilon_{i\_d}[n-1]) + K_{integral_{i\_d}} T_s \varepsilon_{i\_d}[n]) \quad (5.11)$$

$$V^*_{q_m}[n] = V^*_{q_m}[n-1] + K_{p_{i\_q}}(\varepsilon_{i\_q}[n] - \varepsilon_{i\_q}[n-1]) + K_{integral_{i\_q}} T_s . \varepsilon_{i\_q}[n]) \quad (5.12)$$

Here, the term ε_{i_d} refers to the error, which is calculated by subtracting $I_d$from$I_{d_{ref}}$, where as ε_{i_q} denotes the error, computed by subtracting I_d from $I_{q_{ref}}$.The reference PV inverter voltage signal for the d-axis and q-axis are represented by the symbol $V^*_{d_m}[n]$ and $V^*_{q_m}[n]$ respectively. The proportional and integral gains of the d-axis current regulator are denoted by the variables $K_{p_{i\_d}}$ and $K_{integral_{i\_d}}$, respectively The proportional and integral gains of the q-axis current regulator are denoted by the variables $K_{p_{i_q}}$and$K_{integral_{i_q}}$, respectively.

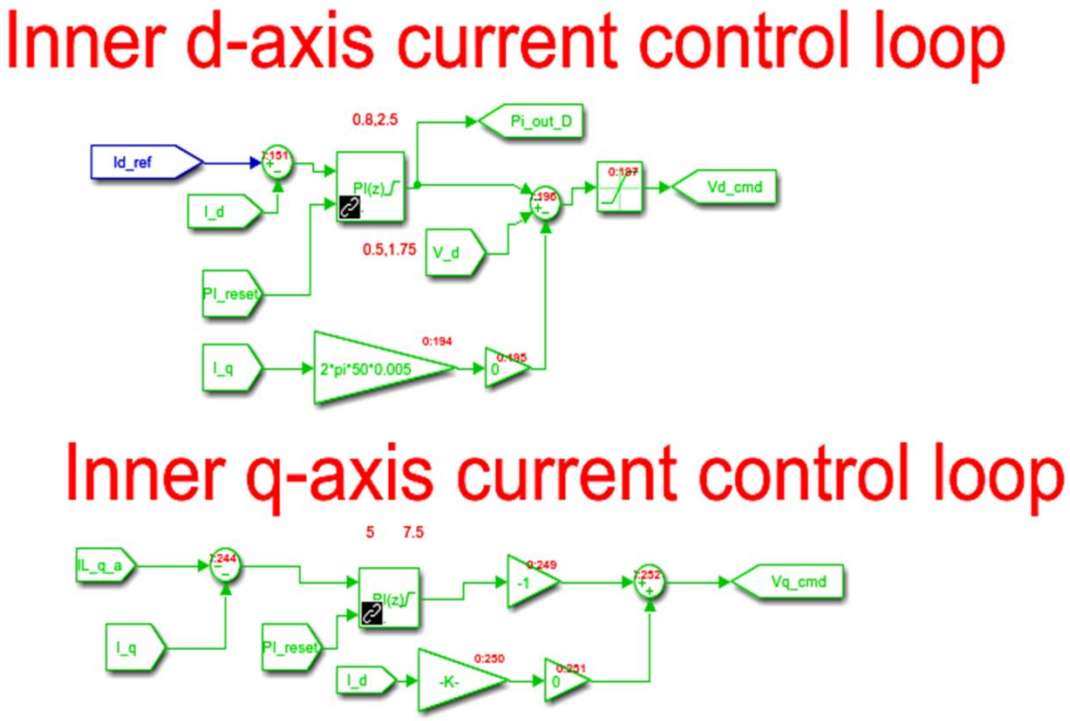


Figure 5-15: Configuration View of synchronous frame inner current control loop

It is possible to derive the modulating PV inverter voltages in a synchronous frame by taking the internal decoupling into account. It is expressed as follows:

$$V_{d_m}^{*}[n] = V_d[n] - V_{d_{ref}}^{*}[n] + I_q[n] \times \omega[n] \times L \quad (5.13)$$

$$V_{q_m}^{*}[n] = V_q[n] - V_{q_{ref}}^{*}[n] - I_d[n] \times \omega[n] \times L \quad (5.14)$$

Equation (5.13) to (5.14), which contain the values of $V_{d_m}^{*}[n]$ and $V_q^{*}[n]$, are realized in target Simulink model with sampling timeT_s, which is indicated by green color. The inner current loop of multipurpose PV system (as depicted in Figure) is tested and validated experimentally. The steady state performance of current control loop in synchronous reference frame is carried out by taking three test cases such as : (i) only active current injection ($i_{inverter(ref)_d}$= -2 A and $i_{inverter(ref)_q} = 0$,Conventional PV system), (ii) active current injection and reactive power exchange ($i_{inverter(ref)_d}$= -2 A and $i_{inverter(ref)_q} = +1.5/-1.5$, Partial PV-STATCOM system), and (ii) only reactive power support ($i_{inverter(ref)_d}$= 0 and $i_{inverter(ref)_q} = +1.5/-1.5$, Partial

Full-STATCOM system). In the first test case, the real power is injected into the grid by PV inverter. During experiment in a day time, the reference value of DC-bus ($V_{dc_{ref}}$) is set to 240V and PV current is observed 1.8 A . The reference value of d-axis is generated as per the equation and given to d-axis inner current control loop. While the reference value of q-axis is set to be zero. The line to line voltage of PCC is adjusted at 110 V (rms value). It is noted from the figure 5-16 that active current of 2A is only injected into utility. The PCC voltage and inverter current are out of phase, as depicted in Figure5-16. The reactive power support is not provided by PV inverter, as observed from the Figure 5-16.

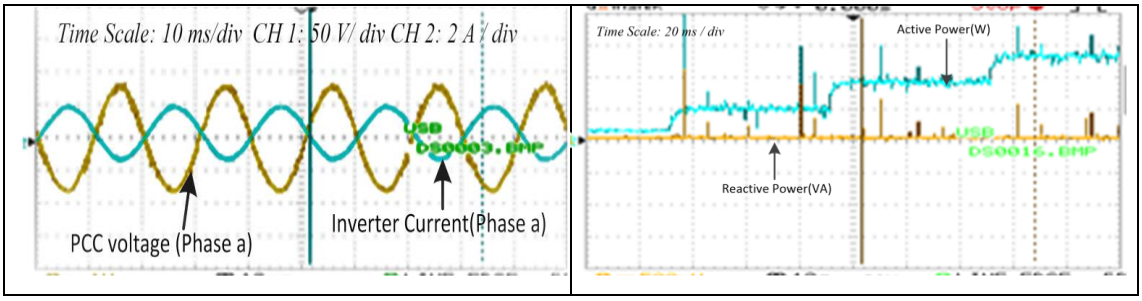
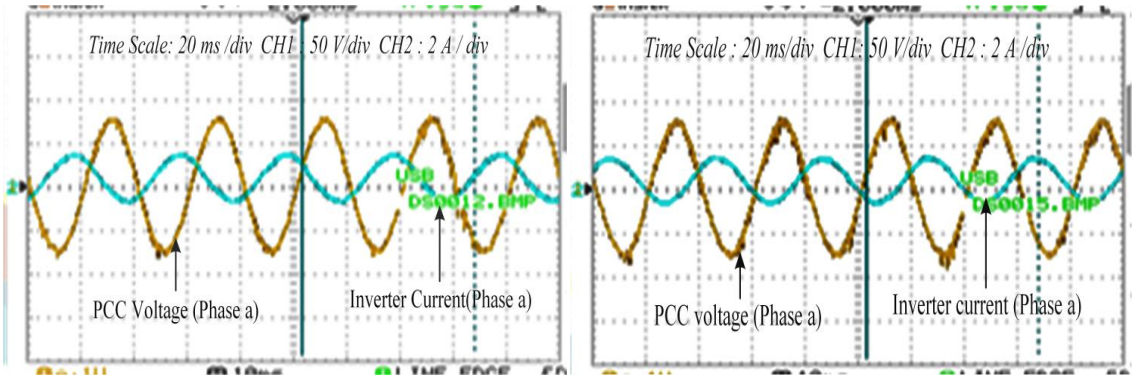


Figure 5-16: Experimental results of inner current control loop obtained in grid-tied PV system without outer voltage controller by taking $i_{inverter(ref)_d}$= -2 A and $i_{inverter(ref)_q} = 0$, Conventional PV system

During second test case, the active power injection and reactive power exchange by the of multi-purpose PV inverter is validated its effectiveness by utilizing a remaining capacity of PV inverter. The reactive power support provided by multi-purpose PV inverter when inductive or capacitive load is connected at PCC to maintain unity power factor at the utility grid. The active power injection is managed by MPPT algorithm as per the availability of solar irradiance from dawn to duck. The reactive power support i.e. Partial-STATCOM is demonstrated by considering two cases: inductive mode and capacitive mode operation of PV inverter. Instead of capacitive load or Inductive Load, the reference value of d-q axis load current value is chosen a fix value i.e. $i_{inverter(ref),d}$ and $i_{inverter(ref),q}$ for an experimental validation. Therefore, PCC voltage (Phase a) and inverter current (Phase a) are observed as experimental result to conclude the nature of PV system. If the inverter currents are lagging to PCC voltages with the chosen fix d-q axis capacitive load

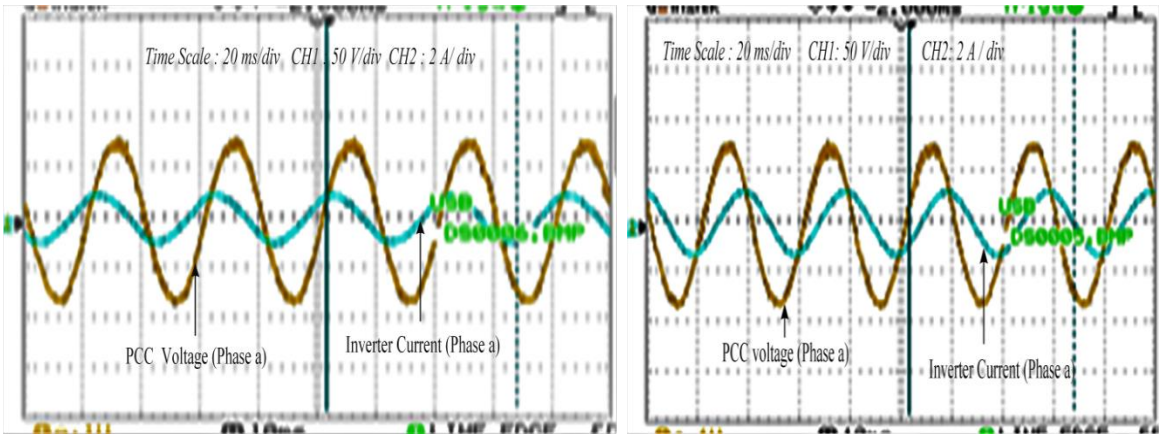
current value, then inductive nature of PV inverter whereas leading to PCC voltages with a chosen a fix d-q axis inductive load current value, then capacitive nature of PV inverter. According to the equation, if capacitive load is connected at PCC at that time PV inverter has to behave as inductive load for maintaining unity power factor at source side or utility grid side, and vice versa. The capacitive behavior of PV system along with active power injection is validated experimentally by taking $i_{inverter(ref)_d}$= -2 A and$i_{inverter(ref)_q} = +1.5$, as depicted in Figure 5-17(a).



(a) (b)

Figure 5-17: Experimental results of inner current control loop obtained in grid-tied PV system without outer voltage controller obtained by taking (a) $i_{inverter(ref)_d}$= -2 A and $i_{inverter(ref)_q} = +1.5$, and (b) $i_{inverter(ref)_d}$= -2 A and $i_{inverter(ref)_q} = -1.5$, Partial PV-STATCOM

The inverter current (Phase A) is leading the PCC voltage (Phase A) to act as capacitive for the compensation of reactive power in inductive load, which fulfil the objective of unity power factor at grid side as STATCOM, as depicted in a Figure 5-17. The inverter current is leading the PCC voltage by observing wave form in the Figure 5-17with respect to the wave form of conventional PV system in figure 5.16. Furthermore, the inductive behavior of PV system along with active power injection is validated experimentally by taking $i_{inverter(ref)_d}$= -2 A and$i_{inverter(ref)_q} = -1.5$, as depicted in Figure 5-17(b). The inverter current is lagging the PCC voltage by observing waveform in Figure 5-17 with respect to the wave form of conventional PV system in Figure 5-16. The inverter current (Phase A) is lagging the PCC voltage (Phase A) to act as inductive for the compensation of reactive power in capacitive load, which fulfil the objective of unity power factor at grid side as STATCOM.



(a) (b)

Figure 5-18: Experimental results of inner current control loop obtained in grid-tied PV system without outer voltage controller obtained by $i_{inverter(ref)_d}$= 0A (a) $i_{inverter(ref)_q} = +1.5$, and (b) $i_{inverter(ref)_q} = -1.5$, Full -STATCOM

The objective of third test case is to provide only reactive power support to the grid. It operates to fulfil prioritize two objectives: 1) voltage control and Power factor correction. If the PCC voltage within acceptable limits, then PV inverter is providing only unity power factor at grid. As per load convention for grid connection, if PV system(here, it is considered as load) is injecting power in grid at that time grid current and PCC voltage out of phase at no-load or resistive load condition while grid current and PCC voltage are in phase when PFC mode(as rectifier) is enabled, when PV panels is disconnected from PV inverter. The PCC voltage is reduced when inductive load connected while increased when capacitive load is connected at PCC. The objective of PCC voltage controller block is to create the reactive current reference according to reference value of PCC voltage. If PCC voltage increases due to capacitive load, multipurpose inverter is acting as an inductor, as shown in Figure in the Figure 5-18(a) , while decreasing at that moment behave as capacitor, as shown in the Figure 5-18(b), to regulate PCC voltage.

5.2.2.8 PWM generation, Display unit, and Protection unit in WAIJUNG block-set

The voltages ($V^*_{d_m}[n]$, $V^*_{q_m}[n]$) are converted to stationary reference voltages ($v^*_{a_m}$, $v^*_{b_m}$, $v^*_{c_m}$) using the following formula:

$$\begin{bmatrix} v^*_{a_m}[n] \\ v^*_{b_m}[n] \\ v^*_{c_m}[n] \end{bmatrix} = \frac{1}{v_{d[n]}} \begin{bmatrix} \sin(\theta_{PLL}[n]) & \cos(\theta_{PLL}[n]) \\ \sin(\theta_{PLL}[n] - \frac{\pi}{3}) & \cos(\theta_{PLL}[n] - \frac{\pi}{3}) \\ \sin(\theta_{PLL}[n] - \frac{2\pi}{3}) & \cos(\theta_{PLL}[n] - \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V^*_{d_m}[n] \\ V^*_{q_m}[n] \end{bmatrix} \quad (5.15)$$

Advance PWM Timer 8 of STM32F407VG microcontroller is used to compare the modulating PV inverter voltages ($v^*_{a_m}[n]$, $v^*_{b_m}[n]$, and $v^*_{c_m}[n]$) to a high frequency carrier wave. The Advance Timer 8 of microcontroller can generate gating pulses using bi-polar sinusoidal pulse width modulation.

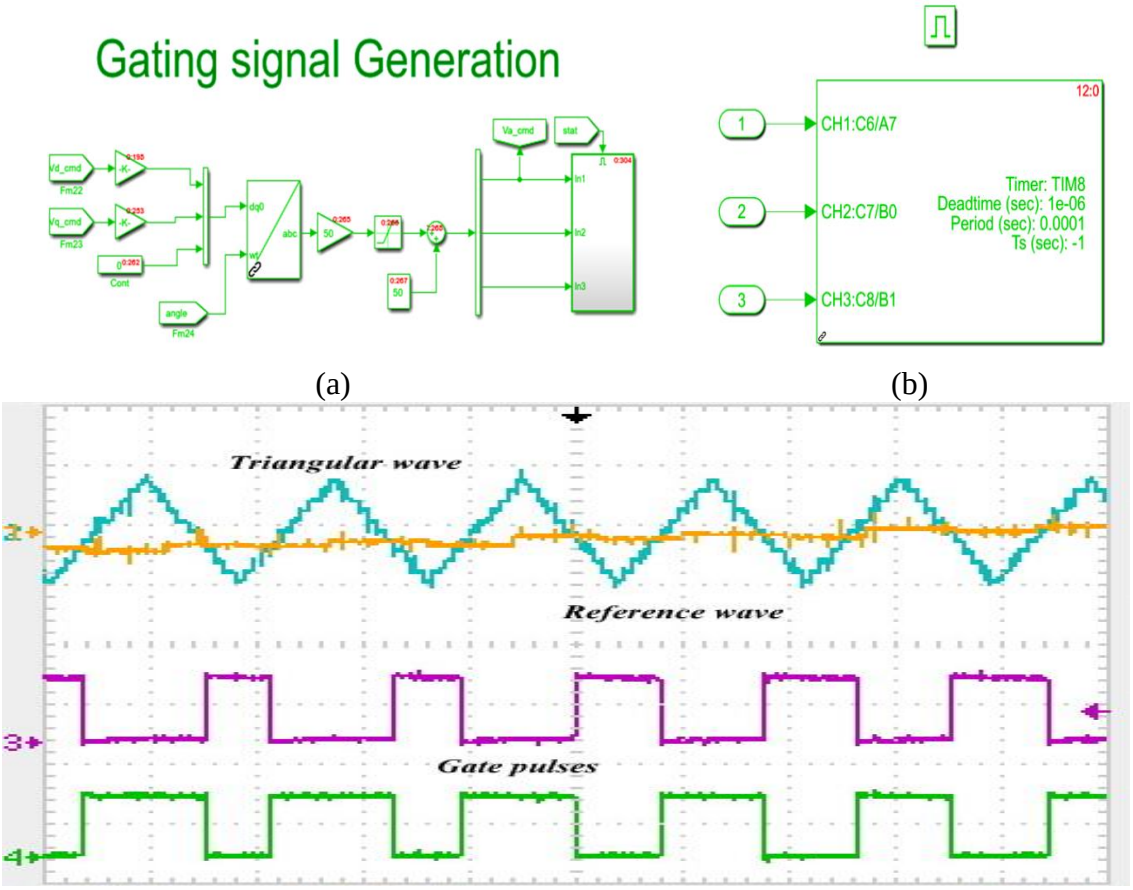


Figure 5-19: Configuration view of PWM generation block in target Simulink file

The modulating signals of PV inverter voltages ($v^*_{am}[n]$, $v^*_{bm}[n]$, and $v^*_{cm}[n]$) are amplified by gain value 50 , and the further added DC offset of value 50, aforementioned modulation technique. Consequently, the signal can vary between 0 to 100 values, which is the duty cycle requirement of Advance PWM Timer in microcontroller, as depicted in Figure 5-19. Active and reactive power control can achieved through the use of the sine pulse width modulation pulses generated by the PV inverters.

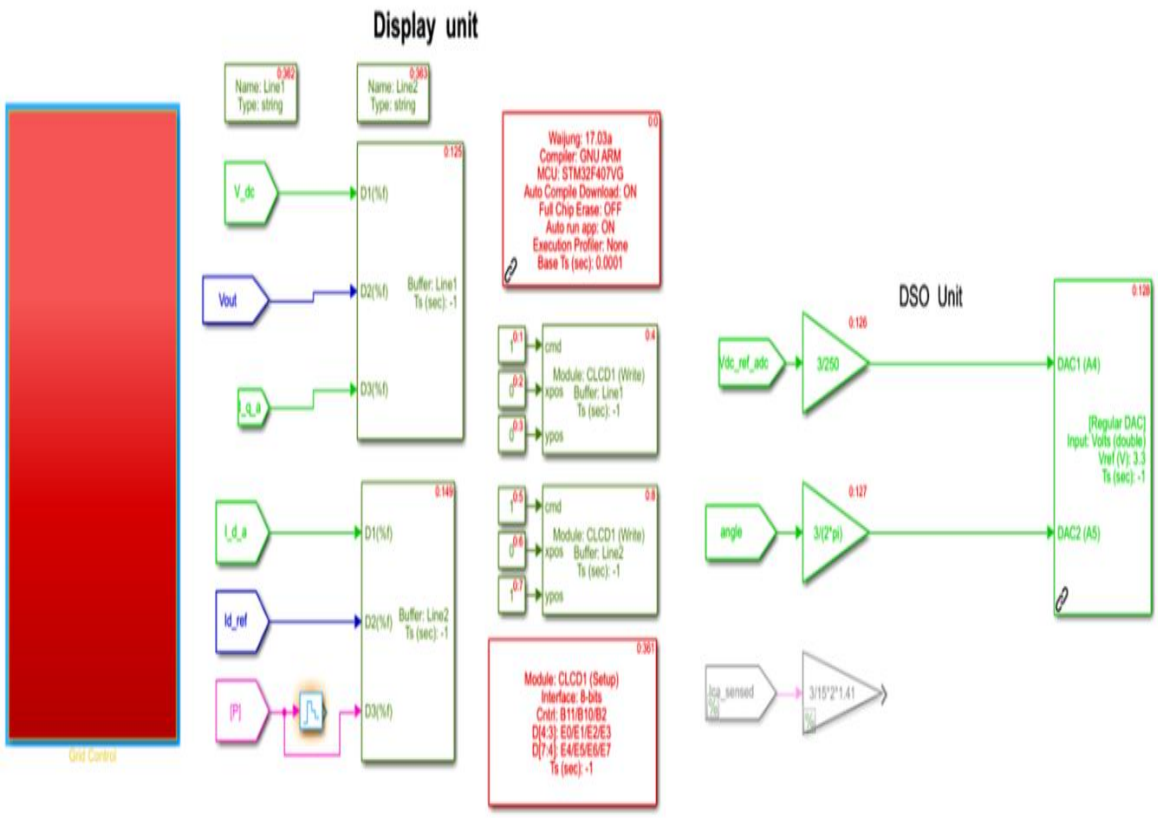


Figure 5-20: Configuration view of Display unit and DSO unit in target Simulink file

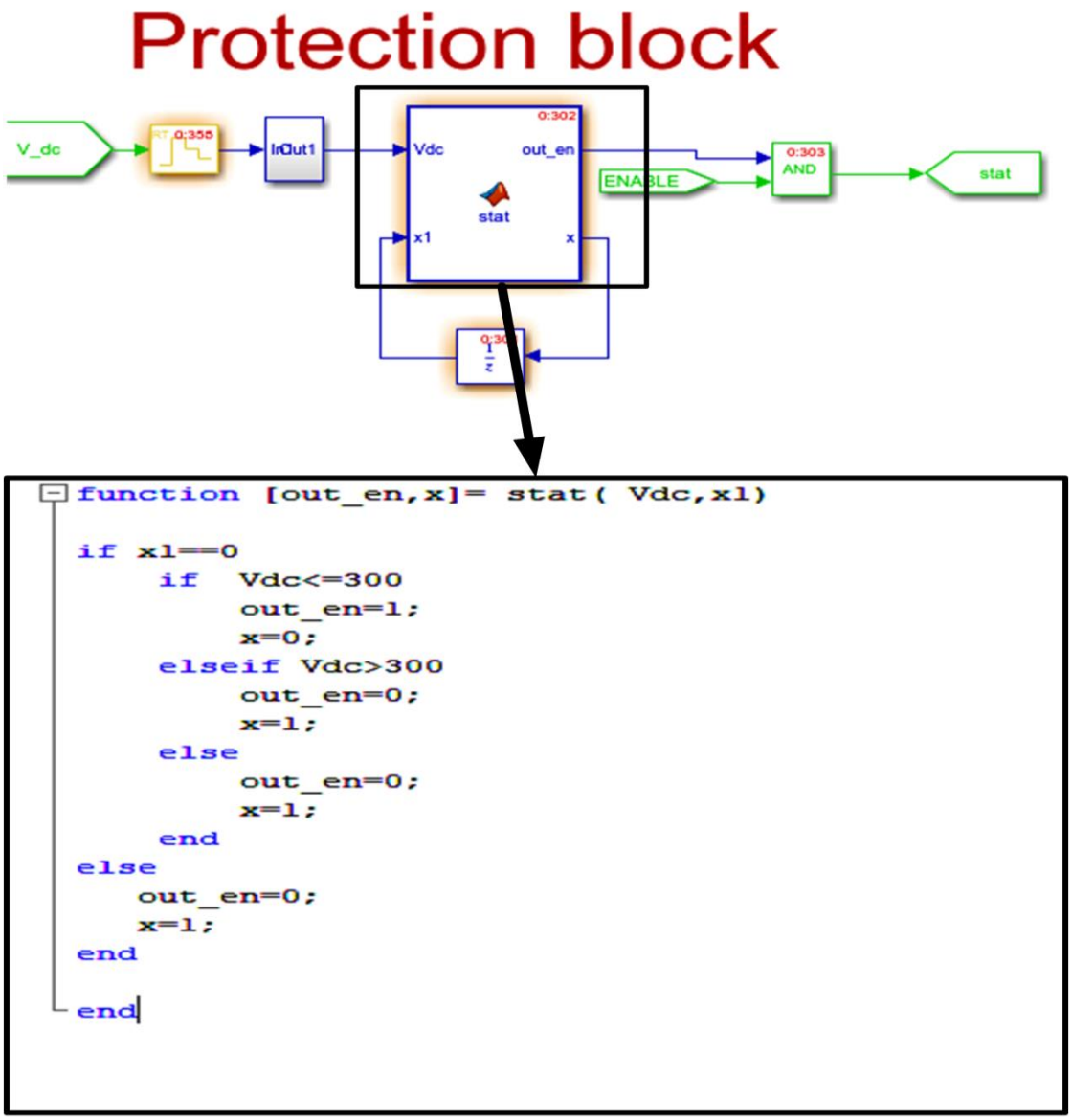


Figure 5-21: Configuration View and m-file Protection algorithm of system

The advance Timer 8 can generates six complimentary PWM gating pulses with programmable dead time insertion (1 micro-second) for the converter through controller pins (C6/A7, C7/B0, and C8/B1), which provides short circuit protection in power card. A Display unit is very crucial during PI controller tuning in outer voltage control loop as well as inner current control loop. The LCD (16*2) setup block is configured in target Simulink file, which have information about microcontroller pins interfaced with command line(RS , read, and write pin) and date

pins(8 bit mode or 4-bit mode). There are two CLCD write block (for line 1 and line 2 in LCD (16*2)) configured in target Simulink , which is used to control character print position for line 1 and line 2.Buffer block is configured to display the quantities which want to be observed during functioning of experimental set-up. A protection block is created to protect the voltage source converter. During operation of grid tied PV system, if DC-bus voltage is out of voltage range ($V_{dc} \leq 300V$), then this block stop the gating pulses from the advance PWM Timer, as depicted in Figure 5-21.

5.3 Experimental setup of the Multipurpose Single-stage grid tied PV system

This chapter describes the laboratory setup and justification of the sensible PV system performance for all three operational modes as a multipurpose PV system. For designing low rating prototype, a 10KVA 3 phase variac (Star/Star configuration) as interface transformer is employed as interconnection of the photovoltaic system, grid, and load at power common coupling. An experimental setup consists of a three phase IGBT power converter card, IGBT driver card with short-circuit protection, STM32F407VG 32-bit DSP based microcontroller, current and voltage Hall sensor for DC side, 3 set of current transformer (CT) and power transformer (PT) for ac side along with the features of DC offset adjustment for uni-polar ADC in a microcontroller, line inductor, 8 series connected PV panel strings, and 3-phase varic as power interface between PV system and utility grid. The inverter currents and PCC voltage are sensed and scaled into proportionally within 3V by 3-set of current transformer (CT) and power transformer (PT)and scaling circuits, respectively. It is to be taken care that microcontroller has uni-polar ADC pins with the limitation of maximum voltage 3.3V at ADC pins. Hence DC offset circuits are required to converter bi-polar signal into unipolar signal. The role of sensors circuit is sensed as well as scaled into 3V (for the safety) and DC offset circuits add 1.5V DC into scaled ac signals to make unipolar signal, which is given to the ADC pins of microcontroller The hall sensors are used to measure current and voltage of PV strings and scaled into 3V to be used in MPPT algorithm to generate active current reference for the control approach of presented PV system. The

discrete model of control system of presented PV system is designed using WAIJUNG block set for STM32F4 series controller in Simulink/MATLAB environment. Simulation models can be easily and automatically converted to C code using the WAIJUNG block-set in Simulink, which can be used to create code for a STM32F family microcontroller models (Targets). The WAIJUNG block-set was created to work with ST Microelectronics high-performance and DSP-capable STM32F4 microcontrollers (STM32F4 Target).

5.4 Experimental Results and Discussion

In this section, the results of experimental study are demonstrated for Partial and Full STATCOM operating modes of multipurpose single-stage PV inverter. The control objectives are power factor correction,voltage control and reactive power control for partial STATCOM mode whereas the objective is voltage control for full STATCOM mode. In Figure 5-22, the experiment setup is depicted as a line diagram. The autotransformer adjusts the 415 V, 50 Hz three-phase line to line voltages to 110 V. Line inductance of 5 mH is coupled to this 150 V grid supply to realize the transmission line. Additionally, the single-stage PV inverter and the load bank are all connected to the PCC via a line inductance terminal. An IGBT inverter with three phases and two levels and a 1920 W SPV source make up the PV inverter. An Agilent 4-channel digital signal oscilloscope is used to record the outcomes of the tests. The DC-bus voltage, grid voltage, load current, and SPV current are all sensed using hall effect-based sensor cards. The three-phase current transformer sensor cards are used to monitor the currents in the PV inverter Experiment setup photos are presented in Figure 5-23.

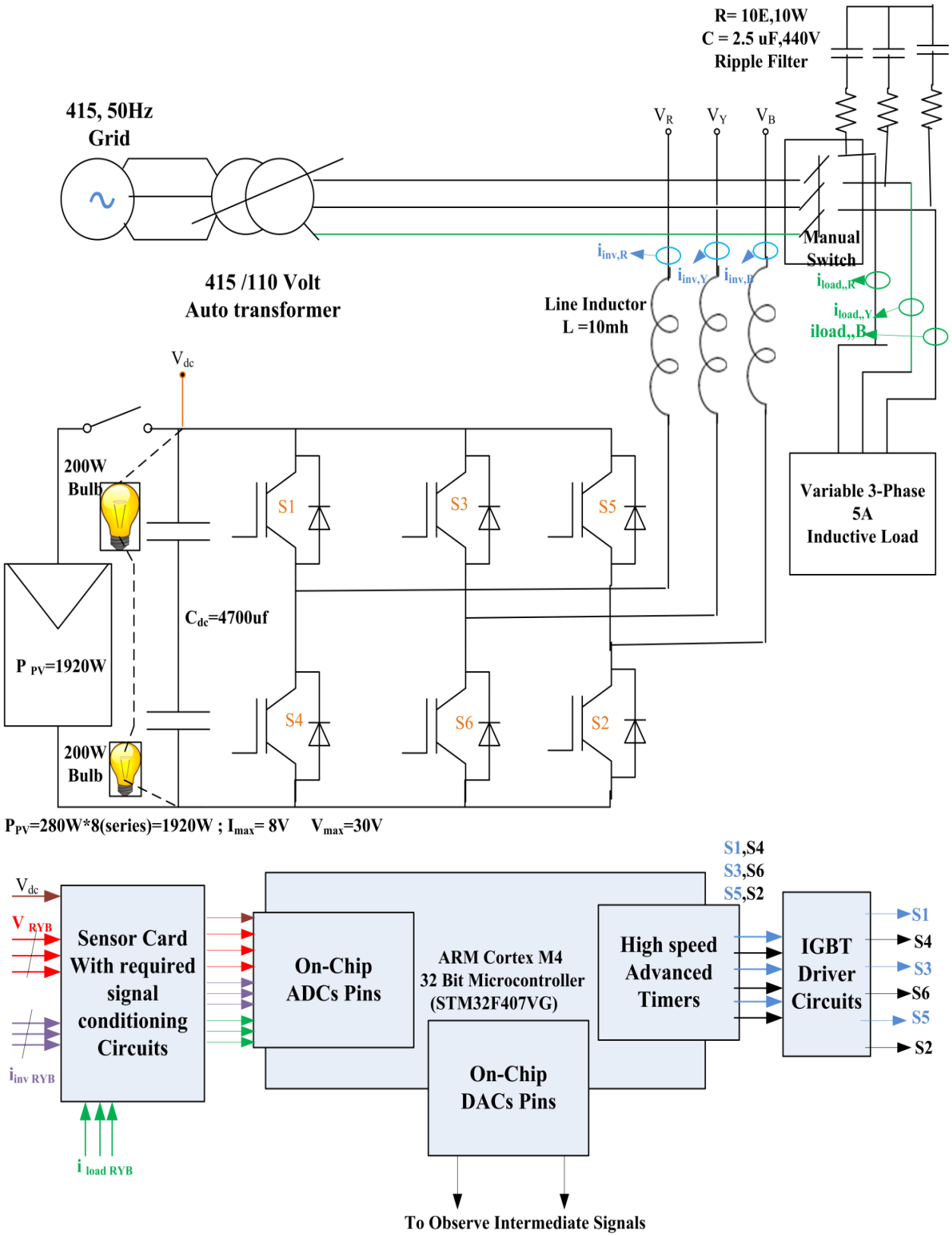


Figure 5-22: Schematic of experimental set-up of Single Stage grid tied PV system

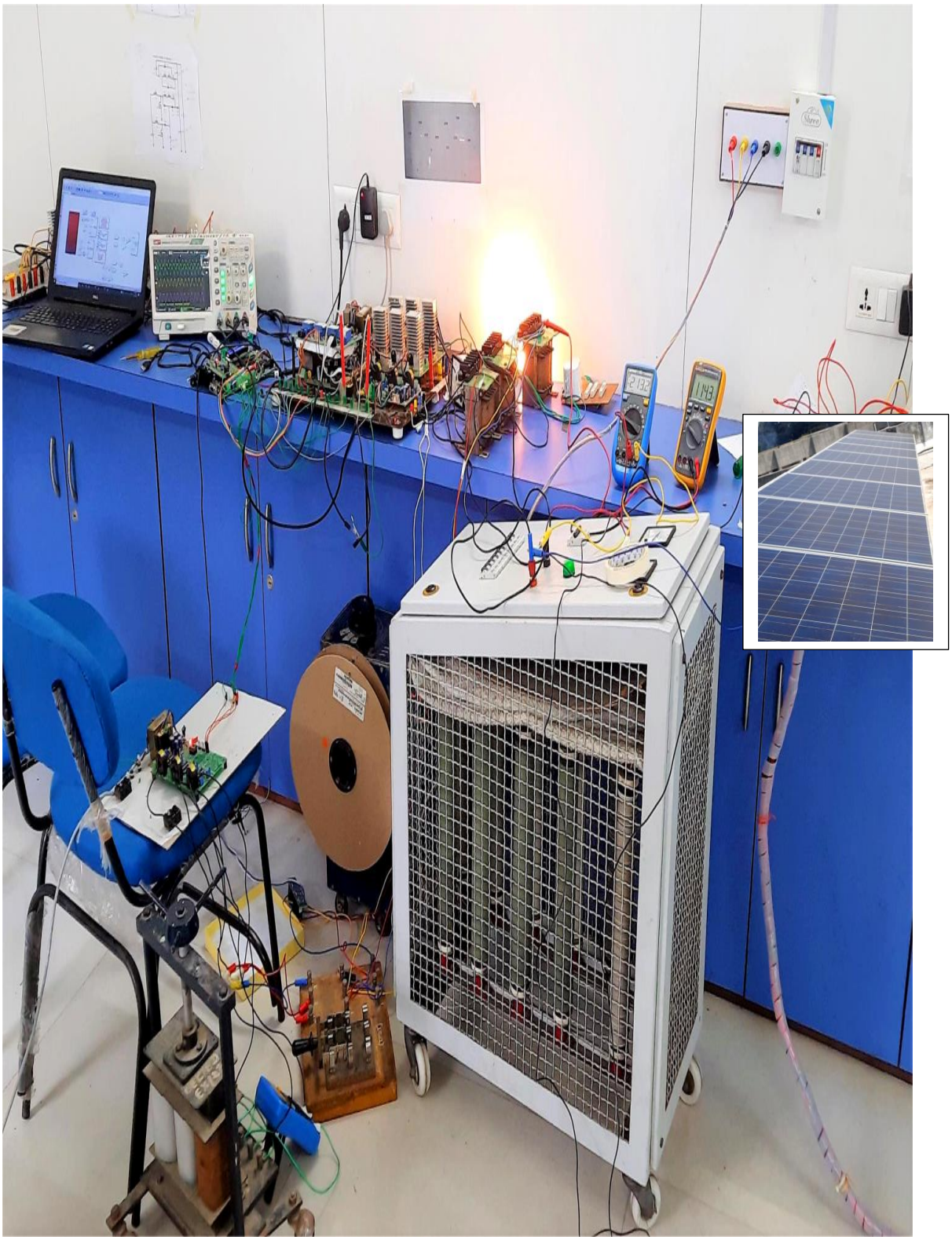


Figure 5-23: Experimental set-up of Single Stage grid tied PV system

TABLE 5-1: PV PANEL AND CONVERTER SPECIFIACTIONS

	Parameter		Value
Photovoltaic Panels All STC ($1000\frac{W}{m^2}$, AM 1.5 Spectrum, cell temperature 25^0C)	Solar power, $P_{PV_{max}}$,		240W
	Volatge at MPP, $V_{PV_{max}}$,Current at MPP, $I_{PV_{max}}$		30V , 8A
	Open circuit voltage ,$V_{PV_{OC}}$		36V
	Short circuit current ,$I_{PV_{SC}}$		8.9A
	No. of PV panels connected in series and Parallel		8(series), 1
	Maximum Power from Photovoltaic Source		240*8=1920W
DC-link	DC-link voltage		250V
	DC-Link capacitance C1 and C2		4700 μfarad
IGBT Power Ratings	Power capacity		12000W
	Switching frequency for PWM		5000Hz
Line Filter	Line inductor		5 mH
Ripple Filter	Resistor		5 ohm
	Capacitor		10 μfarad
Utility Grid	Line to line voltage at PCC, and frequency		110V, 50Hz
	Auto transformer (line to line voltage , and current)		415V/110V, 15 A
Load at PCC	Three- phase variable Inductive Load (delta connected)		0-10A
Control Parameter	**MPPT Control Parameter**	Sampling Time	0.4 seconds
		Step sizeΔ	0.5 Volt
	Modified SOGI-FLL Parameter	Gain($A_{Gain_{DC-Blocker}}$)	0.998
		k_{SOGI} , Γ_{FLL}	0.5 , -1000
		Sampling Time	400 µsecond
	Outer DC-Link voltage Controller	$K_{p_{DC}}$, $K_{integral_{DC}}$	0.5, 3
		Sampling Time	4000 µsecond
	Outer PCC voltage	$K_{p_{PCC}}$, $K_{integral_{PCC}}$	0.5, 3

	Controller	Sampling Time	4000 μsecond
	Inner d-axis current Controller	K_{p_d}, $K_{integral_d}$ Sampling Time	5, 10 400 μsecond
	Inner q-axis current Controller	K_{p_q}, $K_{integral_q}$ Sampling Time	5, 10 400 μsecond

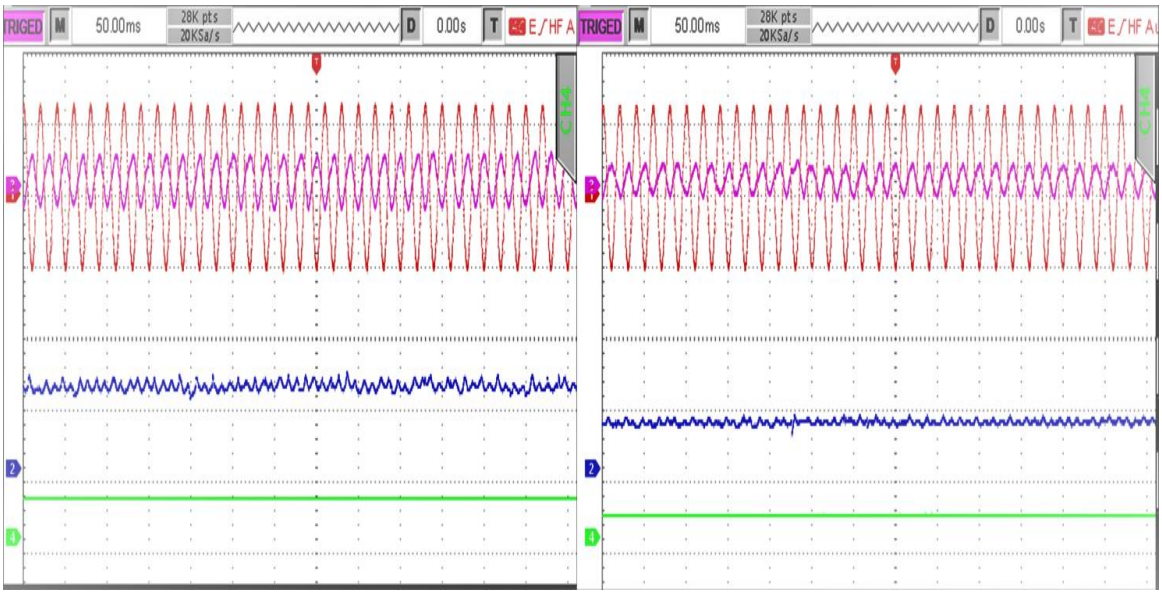
5.4.1 Performance of the multipurpose single-stage grid tied PV system

To monitor the influence of the control system actions on the PCC voltages and source currents, a phase-A of PCC voltage(v_{PCC_a}), source current (i_{source_a}), PV inverter current ($i_{inverter_a}$),and load current(i_{Load_a}), are monitored in the experimental setup. To achieve a desired operation of the presented control system, additional signals such as the DC-bus voltage, PCC voltages, inverter currents, and load currents are sensed. These signals are sent into the ADC pins of a generic ARM CortexM4 microcontroller (STM32F407VG), on which the control system(discussed in chapter 4) is implemented. A sampling time of the MPPT technique is set at 0.4 seconds in the controller. Therefore, the $V_{dc_{ref}}$ is generated for outer voltage control loop every 0.4 second by MPPT block of target Simulink code. The outer voltage control for DC-bus voltage and PCC voltage control are carried out in 4000μs, whereas the inner current control loops through synchronous reference frame are carried out in 400 μs. The grid synchronization block is operated at 400 μs. The outer control loops for DC-bus voltage and PCC voltage control are carried out in 4000 μs, whereas 5KHz is the frequency at which the inverter switches work. The initial PI controller values are computed by considering second ordered control system with damping factor, 0.707. The "Simulink Design Optimization" package of MATLAB is used to further enhance the performance of PI controller using the gradient descent technique [24,25]. The active Solar PV source, which consists of eight 250 W solar panels connected in series, has been thoroughly investigated. Using the modified DSOGI-FLL scheme, the effective grid voltage angle estimate ($\theta_{v_{PLL}}$) is tested, as a

first test of grid- tied multipurpose PV system, and dynamic results are presented in the section 5.2.1.5. A control system of PV inverter is responsible for supplying both active and reactive power to PCC. In addition to active solar power transfer, the PV inverter exchanges the reactive power required by the load, ensuring that the unity power factor operation is maintained at the PCC. According to KCL, the utility grid acts as a source of power for the purpose of determining current direction, whereas the load and the inverter, in the absence of a PV system or a DC source, act as a load by accepting current from the utility grid. The load current is 90^{o} behind the PCC voltage when there is just an inductive load connected to the PCC. The load current is 90^{o} ahead of the PCC voltage (leading) when there is only a capacitive load. Instead of an inductive or a capacitive load attached to PCC, if the voltage source converter is connected to the PCC as a rectifier, the PCC voltages and converter currents (or source currents) are in phase with one another. It has been determined that the utility grid is supplying power to the converter in order to serve as a load convention for current measurement.

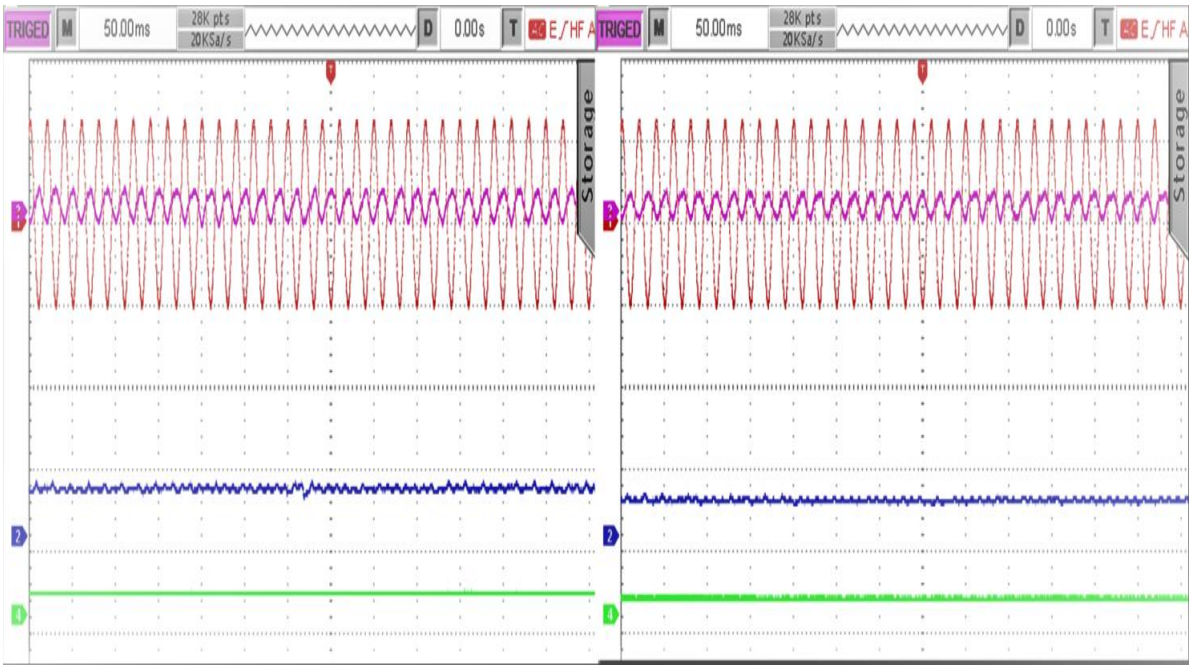
5.4.1.1 Test-1 Steady state performance of multipurpose single-stage PV system using MPPT

The maximum power of solar panel is tracked using a modified DC current sensor-less MPPT technique that is sampled every 0.4 s. The DC-bus voltage is dynamically adjusted to extract maximum power from solar panel, which can be achieved by providing reference DC voltage from MPPT algorithm to outer voltage control loop for active power control. The steady-state and dynamic performance of the power tracking algorithm is evaluated during cloudy day. The performance of modified DC current sensor-less MPPT technique is evaluated by observing v_{PCC_a},i_{source_a}, solar power P_{pv}, and the d-axis component of inverter currents ($i_{inverter_d}$). During cloudy day, four experimental results were recorded and demonstrated in Figure 5-24.At 430 $\frac{W}{m^2}$ of solar radiation, the steady-state power tracking performance is shown in Figure 5-24(a).



(a) (b)

Figure 5-24: Dynamic performance of single stage grid tied PV system during variable solar irradiance (Time scale:60ms//div) : v_{PCC} (Red; Scale 75V/div), i_{source} (Pink; Scale: 4A/div), P_{PV} (Blue; Scale: 500W/div), and i_d (green Scale: 4A/div)



(a) (b)

Figure 5-25: Dynamic performance of single stage grid tied PV system during variable solar irradiance (Time scale:60ms//div) : v_{PCC} (Red; Scale 75V/div), i_{source} (Pink; Scale: 4A/div), P_{PV} (Blue; Scale: 500W/div), and i_d (green Scale: 4A/div

To demonstrate the steady-state tracking performance at 430 $\frac{W}{m^2}$ of solar radiation, Figure 5-24(a) provides to get the comparable Solar PV output of 650 watts (W). Both the DC-bus voltage and the d-axis component of inverter currents ($i_{inverter_d}$) are recorded at 232 V and 2.8 A in the system. However, with lower sun radiation (250 $\frac{W}{m^2}$), steady-state power tracking performance is shown in Figure 5-24(b) with a little lower value of DC-bus voltage (205 V), the d-axis component of inverter currents (1.6 A), and generated SPV power (328 W) than at the previous higher sun radiation condition. Figure 5-25(a) shows the SPV power tracking performance as the ambient conditions vary with a slighter higher value of DC-bus voltage (211 V), the d-axis component of inverter currents (1.8 A), and generated SPV power (379W). At lower solar radiation (290$\frac{W}{m^2}$), steady-state power tracking performance is shown in Figure 5-25(b), where the DC-bus voltage (201V), d-axis component of inverter currents (1.3A), and generated solar power are adjusted at somewhat lower values than in the preceding greater sun radiation condition, respectively. It is demonstrated in Figure 5-25. a that the DC-bus voltage is adjusted at the value for extracting maximum power from solar panels through outer voltage control loop of active power control and modified MPPT algorithms, which is injected into the grid. Peak power tracking can be achieved by varying the DC-bus voltage in response to changes in the surrounding environment.

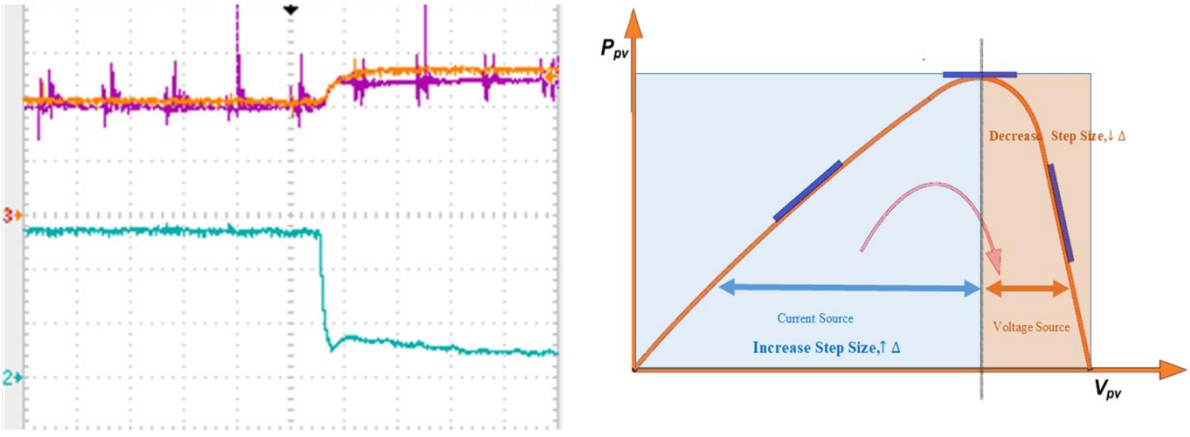


Figure 5-26: (a)Dynamic Performance of DC-bus reference voltage and DC-bus voltage and d-axis current synchronous reference frame. (Time scale:2ms//div) : V_{DC} (purple)and $V_{DC_{ref}}$(orange) : Scale: 110V/div, and i_d (cyan)Scale: 1A/div, and (b) the PV curve characteristics

The source current increases with an increase in Solar PV generation(as increase in solar irradiance), while decreases with decrease in in solar irradiance , as depicted in Figure 5-24 and Figure5-25.The dynamic performance of DC-link outer loop voltage controller is validated by changing DC-bus reference voltage from fix 230 Volt to fix 265V through switching function. The voltage at MPP ($V_{MPP_{solar\ Panels}}$) for panels is 240Volt.The the d-axis component of inverter currents ($i_{inverter_d}$) is decreased from 2.8A to 0.7 A when the DC-bus reference voltage increased from the fix 230 Volt to fix 265V. It is observed from the Figure5-26 that DC-bus voltage is fine-tuned with DC-bus reference voltage. Furthermore, d-axis current is decreased when DC-bus reference voltage is higher than the voltage at maximum power point. A modified DC current sensor-less MPPT is designed as per the observation from Figure5-26(b). If $\Delta I_d > 0$, then $\frac{\Delta I_d}{\Delta V_{dc}} > 0$,and the MPPT reference voltage is increased to bring the operating point towards the maximum power point.

Table-5-2 Possible Variations in Modified DC current Sensor-less MPPT

Cases	$\Delta i_{d_{inverter}}$	$\Delta V_{DC-link}$	$\frac{\Delta i_{d_{inverter}}}{\Delta V_{DC-link}}$	Action Required	Response
Case-I	+ve	+ve	+ve	$\uparrow V_{dc_{ref}}$	$\uparrow P_{PV}$,$\uparrow V_{DC}$
Case-II	+ve	-ve	-ve	$\downarrow V_{dc_{ref}}$	$\uparrow P_{PV}$,$\downarrow V_{DC}$
Case-III	-ve	+ve	-ve	$\downarrow V_{dc_{ref}}$	$\uparrow P_{PV}$,$\downarrow V_{DC}$
Case-IV	-ve	-ve	+ve	$\uparrow V_{dc_{ref}}$	$\uparrow P_{PV}$,$\uparrow V_{DC}$

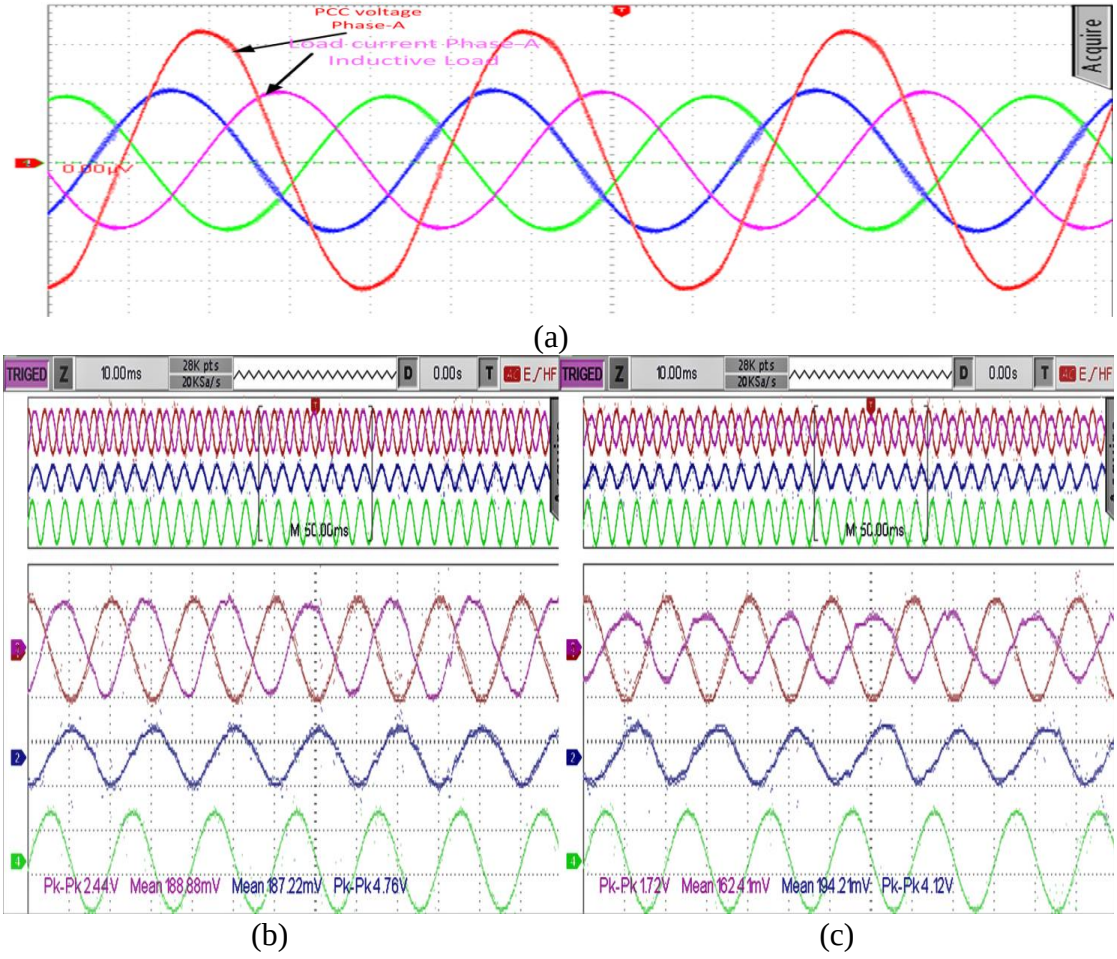
The reference voltage $V_{dc_{ref}}(k)$ for outer voltage control loop is computed by modified MPPT algorithm as per the equation.

$$V_{dc_{ref}}(k) = \begin{cases} V_{dc_{ref}}(k) + \Delta V_{step-size} & (\Delta I_d > 0 \& \Delta V_{dc} > 0) \,||\, (\Delta I_d < 0 \& \Delta V_{dc} < 0) \\ V_{dc_{ref}}(k) - \Delta V_{step-size} & (\Delta I_d < 0 \& \Delta V_{dc} > 0) \,||\, (\Delta I_d > 0 \& \Delta V_{dc} < 0) \end{cases} \quad (5.15)$$

While$\Delta I_d < 0$, then $\frac{\Delta I_d}{\Delta V_{dc}} < 0$,and the MPPT reference voltage must be decreased in order to bring the operating point towards the maximum power point.

5.4.1.2 Test-2 Performance of system as Partial PV- STATCOM

The sensed PCC voltage(Phase-A) and load currents are shown in Figure 5-27(a). .The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). It is noted from Figure 5-27 (b) that the PV inverter is only injecting active power to the grid, and no reactive power support is provided by the inverter during this operation. Figure5-27(b) illustrate the performance indices of v_{PCC_a},i_{source_a}, $i_{inverter_a}$, andi_{load_a}. It is noted that the multipurpose PV system is operated active power injection mode (as conventional PV system) and only inject active power (W)into utility grid at maximum power point using MPPT algorithm on inverter, and further more inverter currents and PCC voltages are 180^oout of phase as depicted in Figure 5-27(b). The PV inverter injects additional power into the utility grid. The active power requirement of inductive load is provided by the photovoltaic inverter and surplus power injected into the grid, while the grid provides the reactive power that is required by the inductive load, as seen in Figure 5-27(b). Figure5-27 (b) illustrates the steady state performances at 240 $\frac{W}{m^2}$solar radiations. In Figure5-27 (b), solar power of 185 W is generated at 240$\frac{W}{m^2}$. The PV inverter has generated 1.8 ampere current in which 1 ampere current is delivered to the variable three phase inductive load and extra 0.8 ampere current is injected to the grid, as depicted in Figure5- 27(c). The DC-bus voltage is adjusted to 230 V which MPP voltage corresponding to is given sun radiation of 240$\frac{W}{m^2}$. As a result, the power factor is noted to be non-uniform, as seen from the Figure 5-27(a). In Figure 5-27(b), the power factor correction mode is activated which means multi-purpose PV inverter is providing reactive power support in addition of active power injection. Figure 5-27 (b) illustrate that PCC voltages and source currents are not maintained at unity power factor where as PCC voltages and source currents are out of phase. The PV inverter current is leading to PCC voltage , whereas load current is lagging to PCC voltage, as depicted in Figure 5-27. It is concluded that multi-purpose PV inverter behave as capacitive load for providing reactive power support to the grid when inductive load is connected at the PCC.



(a)

(b) (c)

Figure5-27:(a) Waveform of sensed Phase-A PCC voltage and sensed three phase inductive load currents, (b)Experimental Results of PV inverter without reactive power support at grid side, and (c) Experimental Results of PV inverter with reactive power support at grid side(Time scale:10ms//div) : v_{PCC} (Red; Scale 75V/div), i_{source} (Pink; Scale: 0.4A/div), $i_{inverter}$ (Blue; Scale: 1.6A/div), and i_{load} (green Scale: 0.5A/div)

The v_{PCC_a} and i_{source_a} are observed to be in out of phase, and the PV inverter current ($i_{inverter_a}$) is noted to be ahead of the power supply voltage, v_{PCC_a} . PV inverters transfer active solar PV power and exchange reactive power required by a three phase variable inductive load as depicted in Figure 5-28(a). As a result of the PV inverter is supplying the three phase variable inductive power demand (active and reactive), the v_{PCC_a} and i_{source_a} are noted to be in- phase, as depicted in Figure 5-28(b).

(a)

(b)

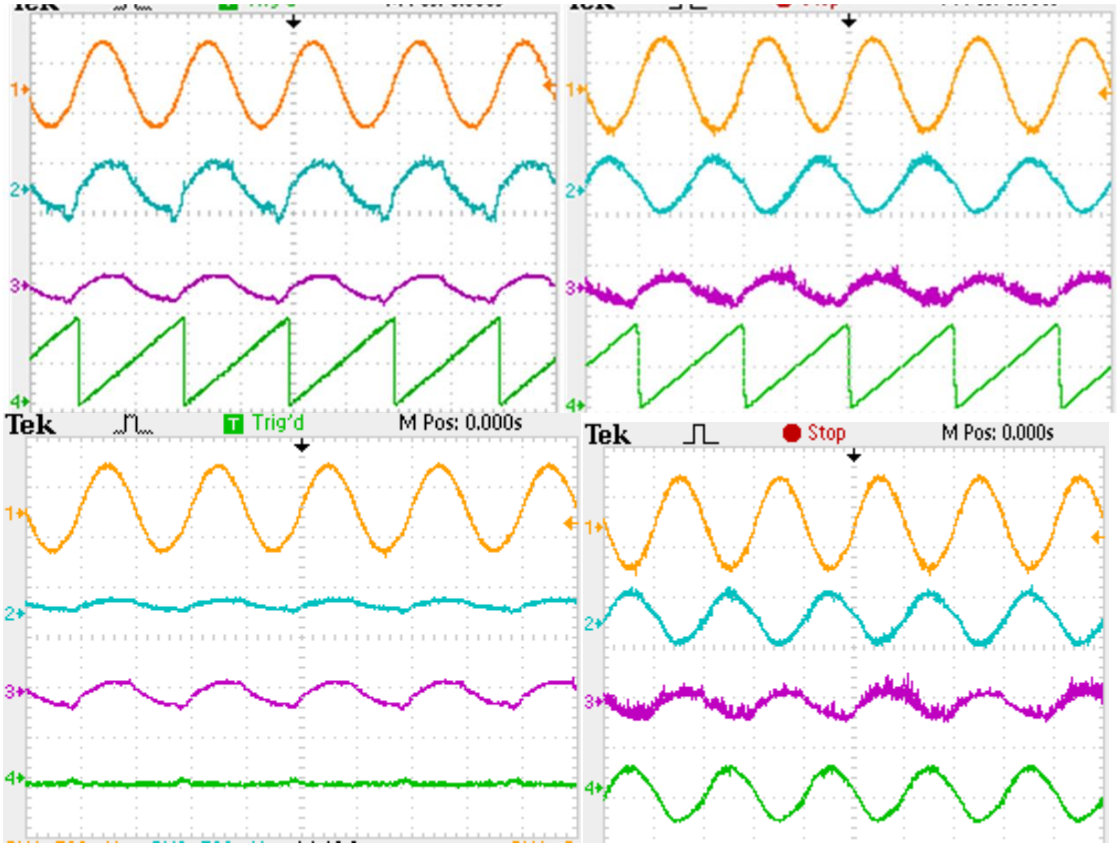


Figure 5-28:Experimental results(Time scale:10ms//div) (a) PCC voltage of Phase-A(Orange; Scale 75V/div), Source current of Phase-A((Cyan; Scale 1A/div), load current of Phase-A(Purple:Scale-2A/div), and grid angle(green), and (b) PCC voltage of Phase-A, Source current of Phase-A, load current of Phase-A, and inverter current of Phase-A(green: scale :2A/div

5.4.1.3 Test-3 Performance of PV system as Full-STATCOM

The power factor is preserved steady at power factor. It demonstrates that the photovoltaic inverter meets load requirements when necessary and sufficient solar power is not available or during night time. Figure 5-29 illustrates the steady state performances during night time. The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). The dynamic performance of the PV inverter is shown in Figure 5-29, when it is attached without and with three phase inductive load and maintained unity power factor at grid (Full-STATCOM Test of multipurpose PV system). The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). Figure 5-28 and Figure 5-29 illustrates the performance of PV system in the unity power factor mode when the load current varies during day time or night time. Full-STATCOM Test of multipurpose PV

system is carried without PV panels for the night time. The reactive power requirement of the load fluctuates dynamically as the load current varies. It is noted that power factor is kept at unity by supporting reactive power from the shunt connected photovoltaic inverter in accordance with load requirements. FFT analysis is carried out in the digital oscilloscope and noted that current harmonics are less than 5%, which complies with IEEE 519 grid code

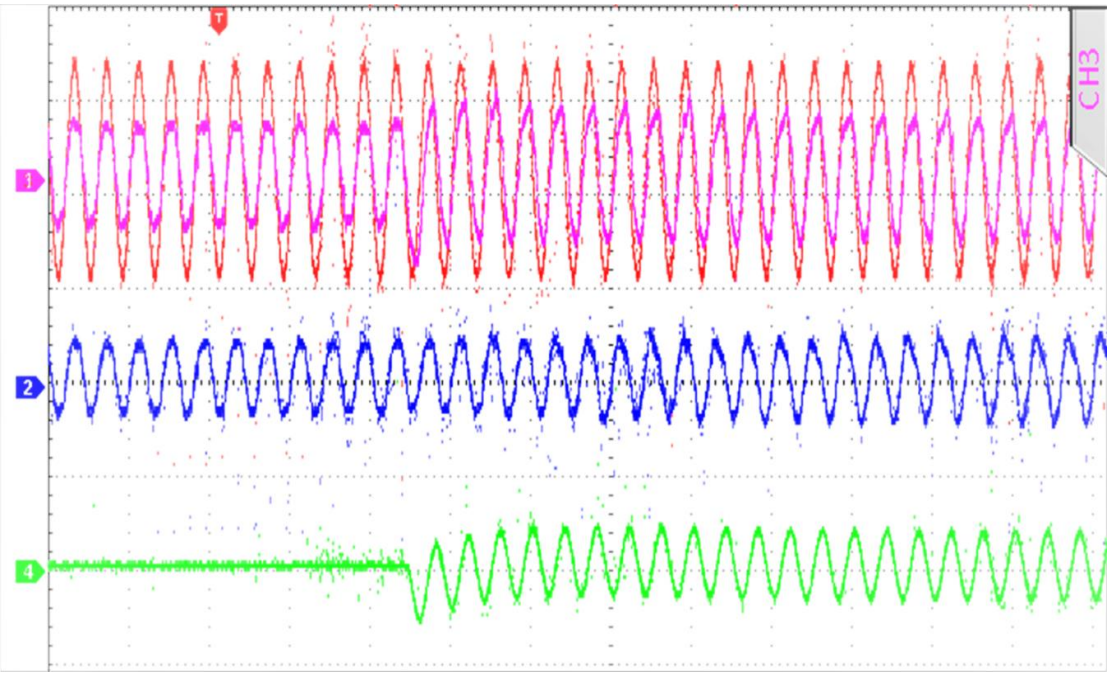


Figure 5- 29: Dynamic results of PCC voltage of Phase-A, Source current of Phase-A, inverter current Phase-A, and load current of Phase-A (Time scale:10ms//div) : PCC voltage of Phase-A(Red: Scale 50V/div), Source current of Phase-A((Pink), load current of Phase-A(Blue), and load current of Phase-A, (green), from no load to inductive load of 1 A

The steady-state performance of the PV inverter is shown in Figure, which is zoom view of Figure 5-30 when three phase inductive load is attached at PCC and maintained unity power factor at grid. Figure 5-29 and 5-30 illustrate the performance indices of v_{PCC_a},i_{source_a},$i_{inverter_a}$, and i_{load_a}. The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). It is noted that multi-purpose PV inverter behave as capacitive load for providing reactive power support to the grid when three-phase inductive load is connected at the PCC. The v_{PCC_a} and i_{source_a} are observed to be in-phase, and the PV inverter current ($i_{inverter_a}$)in Full- STATCOM unity power factor mode is noted to be ahead of the

power supply voltage, v_{PCC_a}.

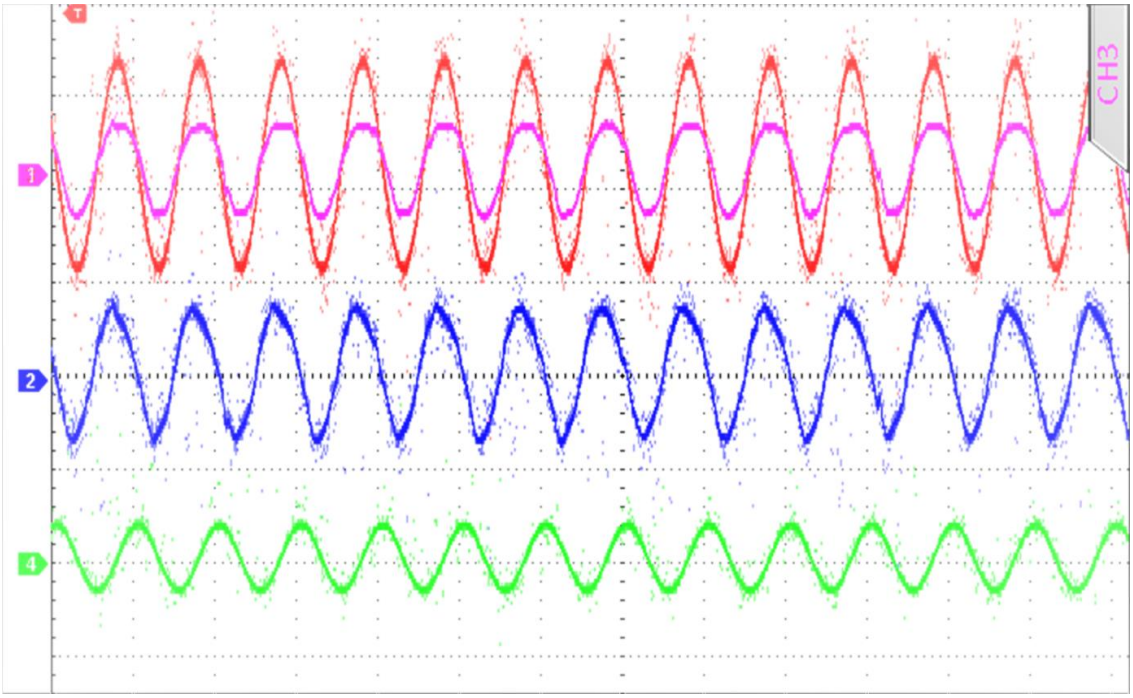
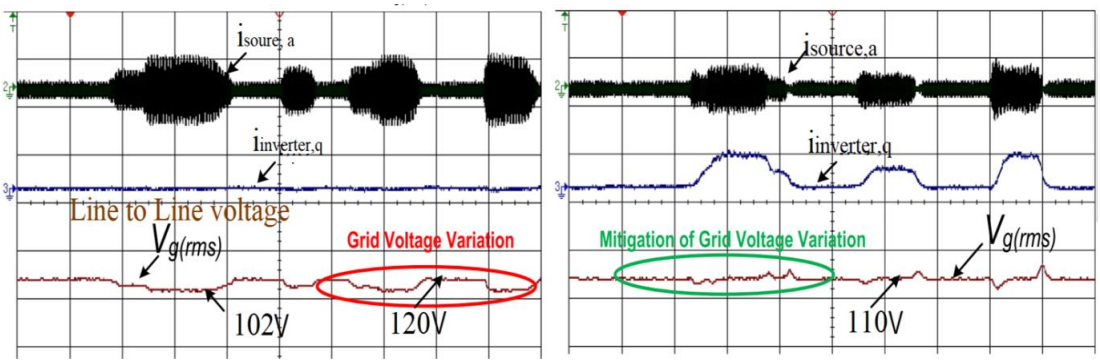


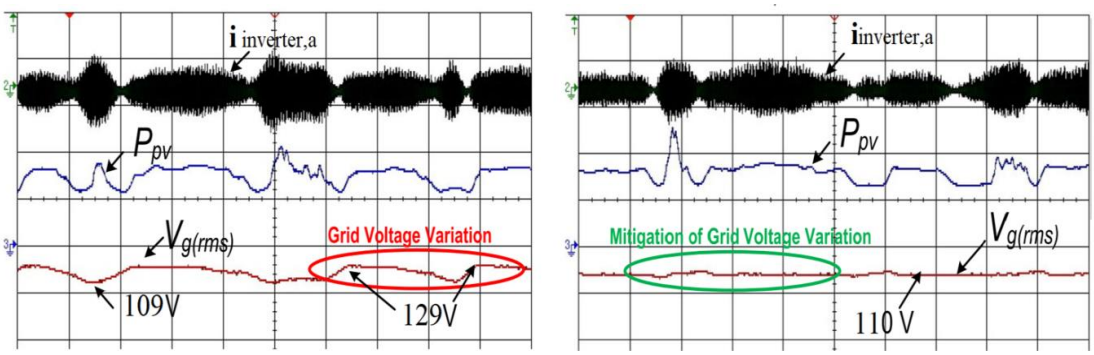
Figure 5-30:Zoom view of Figure 5-29 and experimental results of PCC voltage of Phase-A, Source current of Phase-A, inverter current Phase-A, and load current of Phase-A.

A multipurpose PV inverters exchanges only reactive power which is required by a three phase variable inductive load as depicted in Figure 5-30. A shunt-connected PV inverter is used to support reactive power during this test, which verifies the system's grid voltage management capability. Figure5-31 demonstrates the results of the system with and without grid voltage regulation. Figure 5-31 illustrates how the system performs when the heavy variable restive load connected parallel to the inductive load is adjusted. The supply current (i_{source_a}), the reactive power component of the PV inverter current ($i_{inverter_a}$), and the RMS value of line voltage (v_g), are observed during the experiment. According to Figure 5-31, without grid voltage management, (v_g), fluctuates widely between 102 and 120 V. The reactive power from the PV inverter is supported in Figure 5-31, which reduces the voltage fluctuations. At $110V_{rms}$, the line voltage is kept stable. During a decrease in grid voltage, the leading reactive power is delivered, and vice versa.



(a) (b)

Figure 5-31: Experimental results during PCC voltage control(Source current phase-A, q-axis inverter current , and line to line grid voltage): (a) without PCC voltage control, and(b) with voltage control



(a) (b)

Figure 5-32: Experimental results during PCC voltage control(inverter current phase-A, solar power , and line to line grid voltage): (a) without PCC voltage control, and(b) with voltage control

Figure 5-32 (a) and (b) demonstrate the performance of multipurpose PV inverter with different levels of solar power generation as per solar irradiance. During the experiment, an inverter current ($i_{inverter_a}$), solar power (P_{PV}), and line voltage rms value (V_g) are all measured and depicted in Figure5-32. As can be seen in Figure 5-32, the PV inverter is solely supplying active power to PCC, the grid voltage fluctuates between 102 and 120 V as a result of the dynamic change in SPV power. The performance of the system is illustrated in Figure 5-32(b) when the photovoltaic inverter injects active power and also accommodates reactive power to regulate the grid voltage. The system performs better when the PV inverter also trades reactive power to maintain the grid voltage. Variations in grid voltage are reduced, and the grid voltage is kept constant at 110 volts, as has been seen in Figure 5-32.

5.5 Conclusion

This chapter is validating the multipurpose use of conventional-PV system by modifying control approach to manage the active and reactive power at the utility grid and load side with unity power factor at grid, maintaining PCC voltage is within acceptable range. It has been demonstrated from the experimental results that proposed multipurpose PV system is to inject active power according to solar irradiance and exchange reactive power at PCC to manage either PCC voltage or unity power factor at grid side during day time if and only if PCC voltage within acceptable range. Moreover, it is also proven that it autonomously operated as Full-STATCOM during night time, consequently, grid current remains in unity power factor with PCC voltage when reactive Load is connected to PCC.