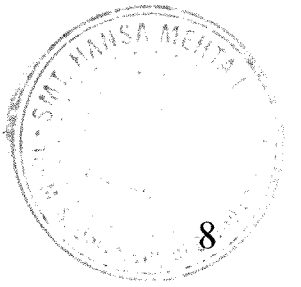
CHAPTER 8

CONCLUSIONS AND FUTURE WORK



8 CONCLUSIONS AND FUTURE WORK

8.1 INTRODUCTION

Internet traffic will continue to grow for many years to come, so there is a great demand for gigabit/terabit electronic routers and switches i.e. IP routers, ATM switches, Ethernet switches. These switches/routers must not only have high throughput but they must support differentiated services, various interface types, scalability port density and multicast support. As line rate increases, more and more applications require the switching system to provide QoS guarantees. In chapter 6 we have introduced, simulated and implemented m-DPA and DSA scheduling algorithms, out of which DSA supports QoS. In chapter 7 we have compared various switching fabrics with iSLIP, m-DPA, and DSA scheduling algorithms for 4x4 and 8x8 switching fabric and experimental results are tabulated. Based on these results following conclusions are drawn.

8.2 CONCLUSIONS

The major conclusions drawn from the results available for MATLAB and VLSI implementations are as follows:

- **Throughput:** From the table 7.1, in 4x4 switches there is 1.5% increase in m-DPA compare to DPA and 3% increase in DSA compare to DPA. From the table 7.3, in 8x8 switches there is 1.2% increase in m-DPA compare to DPA and 2.9% increase in DSA compare to DPA. From the table 7.5, in 16x16 switches there is 0.4% increase in m-DPA compare to DPA and 2% increase in DSA compare to DPA. From the table 7.6, in 32x32 switches there is 0.24% increase in m-DPA compare to DPA and 0.5% increase in DSA compare to DPA. Knockout with L=4 is having highest throughput compared to all. From the simulation results with variation in buffer size, as shown in figures in chapter 6, we can state that there is a significant improvement in throughput in traffic pattern A, C, and D at lower buffer size. As buffer size increases throughput advantage of m-DPA and DSA vanishes.
- **Quality of service (QoS):** From the high QoS DSA simulation results, discussed in chapter 6, we can state that DSA has QoS support level so that packets with higher priority are treated such a way that they have throughput >=99.9%, Average latency <= 0.8, and delay variance <= 7.

- **Latency and Jitter:** From the table 7.1, 7.3, 7.5 and 7.6, average latency of m-DPA and DSA is 0.2, 0.5, 1.25 and 0.5 time slots higher than the DPA in 4x4, 8x8, 16x16 and 32x32 switches respectively. Delay variance in m-DPA is 2, 7, 12 and 55 time slots higher than DPA in 4x4, 8x8, 16x16 and 32x32 switches respectively. Delay variance in DSA is 20, 45, 51 and 190 time slots higher than DPA in 4x4, 8x8, 16x16 and 32x32 switches respectively due to prioritize QoS support.
- **Fairness:** PIM, RRM, iSLIP, RPA, DPA are having good fairness compared to m-DPA and DSA.
- **Speed:** From the tables 7.1, 7.3, 7.5, 7.6 MATLAB simulation time of DSA algorithm is very less compared to DPA, and from VLSI implementation (tables 7.2 and 7.4) operating maximum frequency is significantly higher than DPA. So DSA is fast enough to find a match as quickly as possible.
- **Implementation simplicity:** DSA is possible to implement within a single chip as DPA with 2% more area requirement in 4x4 switch and 5% more area requirement in 8x8 switch.
- **Scalability**: As we go for higher-level switch fabric like 8x8, 16x16, and 32x32 MATLAB simulation time of RPA, DPA and m-DPA are increased drastically but MATLAB simulation time of DSA does not increase like RPA and DPA. Maximum clock frequency of DSA does not decrease like DPA and RPA so it is easily scalable with slightly higher area requirement.
- We have implemented and tested 8 round of IDEA algorithm using Quartus tool in VLSI in EP20k1500EBC652-1 device. IDEA requires 43249 logic elements with maximum clock frequency 3.85 Mhz and 246.4 Mbps data rate. we suggest to add encryption circuitry into the same silicon as the network processor.

8.3 FUTURE WORK

1. The characteristic of the bursty traffic is self-similar in nature which can be modeled as long tailed Pareto distribution. This traffic pattern can be generated and used to evaluate all the algorithms.

2. Generated data using different traffic models in MATLAB can be directly used for test bench verification in VHDL. Once such simulation is carried out, VHDL design can be implemented in FPGA.

3. The work carried out by us can be further extended to enhance DSA, which supports connection oriented and connectionless applications, because a growing trend in next generation network is integration of various protocols, such as IP, ATM and TDM. This work can be further extended to Multiprotocol label switching and optical label switching.

4. Instead of SAMQ buffer, we switch to Dynamic Allocated Multi-Queue (DAMQ) buffer. In DAMQ scheme, virtual queues are allocated dynamically within each input buffer and each virtual queue is maintained by linked list. DAMQ makes buffer usage more efficient, so little modification in DSA makes

it more versatile, in terms of avoid starvation and encourage network fairness. Now, DSA dynamically assigned weight based on summation of latency in the queue, instead of buffer occupancy and prioritized QoS given by the user. Instead of buffer occupancy, we can use threshold of queue latency and table of values of K change as shown in table 8.1:

Table 8.1: Values of K

Case	**K**	**Behavior**
Summation of queue latency < threshold	< 2	Strong capitalistic
	= 2	Fair
	> 2	Socialistic
Summation of queue latency = threshold	> 2	Socialistic and Cautious

5. Instead of speed-up factor N in normal output queuing, same throughput performance can be achieved by using Combine Input Output Queuing. With little modification stable matching concept can be implemented in DSA to incorporate CIOQ.