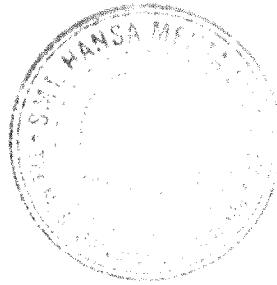


BIBLIOGRAPHY



BIBLIOGRAPHY

1. Agere systems –“Building next Generation Network processors” White Paper April, 2001,
<http://www.agere.com>
2. T. E. Anderson, S. S. Owicki, J. B. Saxe, and C. P. Thacker, “High speed switch scheduling for local area networks,” ACM Transactions on Computer Systems, pp. 319-352, November 1993.
3. Applied Micro Circuits Corporation (AMCC) of <http://www.mmcnetworks.com/> detail of np7xxx, retrieved on June 2004.
4. Peter J. Ashenden, The Designers Guide to VHDL, 2nd Edition, Elsevier, 2004.
5. M. Attia and I. Verbauwhede, “Programmable Gigabit Ethernet Packet Processor Design Methodology”, European Conference on Circuit Theory and Design, Vol. III, pp. 177-180, August 28-31, 2001, Espoo, Finland
6. E. Balaguruswami, Programming in ANSI C, 2.1, Tata McGraw Hill.
7. F. Baboescu and G. Varghese, “Scalable Packet Classification,” in ACM Sigcomm, August 2001.
8. J. Bhasker, A VHDL Primer, 3rd Edition, Pearson Education Asia, 2000
9. D. Chiaroni, C. Chauzat, D. De Bouard, S. Gurib, M. Sotom, J. M. Gabriagues: “A Novel Photonic Architecture for High Capacity ATM Switch Applications”, Photonics in Switching’95, Salt Lake City, Utah, April 1995, paper PThC3
10. H. S. Chi and Y. Tamir, “Decomposed arbiters for large crossbars with multi-queue input buffers” Proc. of International Conference on Computer Design, Cambridge, Massachusetts, October 1991, pp. 233-238.
11. Y. Choi, H. Tode, H. Okada, H. Ikeda: “A Large Capacity Photonic ATM Switch Based on Wavelength Division Multiplexing Technology”, IEICE Trans. Communications, 4 April 1996, vol. E79-B, no.4, pp560-568
12. S. T. Chuang, A. Goel, N. McKeown, and B. Prabhakar, “Matching output queuing with a combined input output queued switch,” Computer Systems Technical Report CSL-TR-98-758, March 1998
13. S. T. Chuang, A. Goel, N. McKeown, and B. Prabhakar, “Matching output queuing with a combined input output queued switch,” Computer Systems Technical Report CSL-TR-98-758, March 1998.

14. Alan Clements, The Principles of Computer Hardware, 3rd Edition, Oxford University Press, 2002.
15. Douglas E. Comer, "Network system design using Network Processor", Pearson Education-2003
16. Alak deb presentation on NP 3, What is a Network Processor?, Vitsee Semiconductor, NetWorld+Interop conference ,Lasvegas 2000, Retrieved on March 2002
17. Benes, V.E., "Optimal Rearrangeable Multistage Connecting Networks," BSTJ, 43(July 1964): 1641-1656.
18. Itamar Elhanany, Kurt Busch, and Derek Chiou, " Switch Fabric Interfaces",IEEE,computer,pp 105-107 September 2003.
19. Itamar Elhanany " A comparative view of the GLIMPS Scheduling algorithms" teracross, October 2002.
20. Itamar Elhanany, O. Beeri "The Glimpse terabit switching engine", February 2002.
21. Ezchip Technologies," 7-layer Packet Processing: A performance Analysis ", White Paper July 2000, www.ezchip.com , retrieved on September 2002
22. Ezchip Technologies," Challenging in designing 40-Gigabit Network Processors", White Paper December 1999,www.ezchip.com, retrieved on September 2002
23. Ezchip Technologies," Network processor Designs for next-generation Networking equipment ", White Paper December 1999, www.ezchip.com
24. A. Feldman and S. Muthukrishnan. "Tradeoffs for packet classification," Proceedings of Infocom, vol. 3, pages 1193-202, March 2000
25. Wajdi Feghali, Gilbert Wolrich,,Douglas Carrigan, Intel Communications Group "High integration makes IPsec fly" An article in EE Times October 14, 2002
26. Behrouz A. Forouzon, Data Communications and Networking, 3rd Edition, Tata McGraw-Hill, 2004.
27. John Freeman, Fearless Group "Changing the Game Winners, Losers, and Opportunities resulting From the Adoption of the Network Processor Unit (NPU), NetWorld+Interop conference ,Lasvegas 2000,Retrieved on March 2002
28. G. Gibson, F. Shafai, and J. Podaima, "Content Addressable Memory Storage Device," United States Patent 6,044,005, March 2000. SiberCore Technologies, Inc.
29. Pankaj Gupta, "Algorithms for routing lookups and packet classification," Dissertation report, Stanford University, December 2000.

30. Pankaj Gupta, Nick McKeown, Packet Classification on Multiple Fields, Proc. Sigcomm, Computer Communication Review, vol. 29, no. 4, pp 147- 60, September 1999, Harvard University
31. Pankaj Gupta, Nick McKeown, Packet Classification using Hierarchical Intelligent Cuttings , Proc. Hot Interconnects VII, August 99, Stanford. This paper is also available in IEEE Micro, pp 34-41, vol. 20, no. 1, January/ February 2000
32. "Hardware Working Group " www.npforum.org/techinfo/charters.shtml
33. R. Handel, M. N. Huber, S. Schroder, "ATM Networks Concepts, Protocols, Applications", 2nd edition, Addison-Wesley
34. Tomas Henriksson, "Intra-Packet Data-Flow Protocol Processor", Licentiate Degree Thesis, Linkoping Studies in Science and Technology, Thesis No. 813, 2003.
35. Tomas Henriksson, Ulf Nordqvist and Dake Liu, "Embedded Protocol Processor for Fast and Efficient Packet Reception", Proceedings of the 2002 IEEE International Conference on Computer Design: VLSI in Computers and Processors (ICCD'02) Freiburg, Germany, September 2002.
36. Tomas Henriksson and Dake Liu, "Implementation of Fast CRC Calculation", Asia South Pacific Design Automation Conference, Kitakyushu, Japan, January 2003.
37. Tomas Henriksson and Dake Liu, "Novel ASIP and Processor Architecture for Packet Decoding", in Workshop of Application Specific Processors Digest, Istanbul, Turkey, November 2002.
38. Tomas Henriksson, "Hardware Architecture for Protocol Processing", Licentiate Degree Thesis, Linkoping Studies in Science and Technology, Thesis No. 911, December 2001.
39. Tomas Henriksson, "In-Line CRC Calculation and Scheduling for 10 Gigabit Ethernet Transmission", Swedish System-on-Chip Conference, Falkenberg, Sweden, March 2002.
40. Tomas Henriksson, Niklas Persson and Dake Liu, "VLSI Implementation of Internet Checksum Calculation for 10 Gigaabit Ethernet", Design and Diagnostics of Electronics, Circuits and Systems, Brno, Czech Republic, April 2002.
41. Tomas Henriksson, Ulf Nordqvist and Dake Liu, "Specification of a Configurable General-Purpose Protocol Processor", Second International Symposium on Communication systems, Networks and Digital Signal Processing, Bournemouth, UK, July 2000.
42. <http://www.ethereal.com/>
43. <http://www.intel.com/design/network/products/npfamily/ixp2350.htm>
44. <http://www.iti.fh-flensburg.de/lang/algorithmen/sortieren/bitonic/bitonicenfra.htm>.

45. <http://www.laynetworks.com/Knockout%20Switch.htm>
46. http://www.mediacrypt.com/_pdf/IDEA_Perf_Overall_0304.pdf
47. <http://www.netfor2.com/>
48. <http://www.networking.ibm.com/314/314prod.html> , detail related to power NP retrieved on December 2002
49. <http://www2.rad.com/networks/1994/ packet-switch-theory/tandban.html>
50. http://www2.rad.com/networks/1994/gbiran/atm_swi.htm
51. J. Hurt, A. May, X. Zhu, and B. Lin, "Design and implementation of high-speed symmetric crossbar schedulers," Proc. IEEE International Conference on Communications (ICC'99), Vancouver, Canada, June 1999, pp. 253-258
52. Intel <http://developer.intel.com/design/network/products/npfamily> ,detail
53. Intel® Corporation, Network Processor Division, " Next Generation Network Processor Technologies, Enabling Cost Effective Solutions for 2.5 Gbps to 40 Gbps Network Services", White paper October 2001
54. Giacopelli, J. N., et al., "Sunshine: A High-Performance Self Routing Broadband Packet Switch Architecture," Proc. XIII Internatl Switching Symposium, ISS 90, Stockholm, May 1990.
55. Hui, J. Y., Switching and Traffic Theory for Integrated Broadband Networks, Boston: Kluwer Academic Publishers, 1990.
56. M. J. Karol, M. G. Hluchyj and S. P. Morgan, "Input vs. output queueing on a space-division cell switch", IEEE Transaction on Communications, Vol. 35, No. 12, pp. 1347-1356, 1987.
57. H. W. Johnson, "Fast Ethernet Dawn of New Network", Prentice Hall
58. Patel, J. H. "Performance of Process-Memory Interconnections for Multiprocessors," IEEE Trans. Computers, C-30, 10(Oct. 1981): 771-780.
59. Aaron Kershenbaum, "Telecommunications Network Design Algorithms", Mc Graw Hill, 1993
60. R. A. Kempke and A. J. McAuley, "Ternary CAM Memory Architecture and Methodology." United States Patent 5,841,874, November 1998. Motorola, Inc
61. Maryam Keyvani, "VHDL Implementation of a High-speed Symmetric Crossbar Switch, " University of Tehran, 1998.
62. Dake Liu, U. Nordqvist, and C. Svensson, "Configuration-Based Architecture for High Speed and General-Purpose Protocol Processing", IEEE Workshop on Signal Processing Systems, Taipei, Taiwan, 1999.

63. A. J. McAulay and P. Francis, "Fast Routing Table Lookup Using CAMs," in IEEE Infocom, 1993.
64. N. McKeown and T. E. Anderson, "A quantitative comparison of scheduling algorithms for input-queued switches," Computer Networks and ISDN Systems, vol. 30, no. 24, pp. 2309-2326, Dec. 1998.
65. N. McKeown, "The iSLIP scheduling algorithm for input-queued switches", IEEE Transactions on Networking, vol. 7, no. 2, pp. 188-201, April 1999
66. N. McKeown, M. Izzard, A. Mekkittikul, B. Ellersick, and M. Horowitz, "The Tiny Tera: A small, high bandwidth network switch," IEEE Micro, January/February 1997, pp.26-33
67. N. McKeown, V. Anamtharam, and J. Warland, "Achieving 100% throughput in an input-queued switch," Proc. INFOCOM'96, San Francisco, March 1996, pp. 296-302
68. A. Mekkittikul and N. McKeown, "A practical scheduling algorithm to achieve 100% throughput in input-queued switches," Proc. IEEE INFOCOM 1998, vol. 2, Apr. 1998, San Francisco, pp. 792-799.
69. A. Mekkittikul and N. McKeown, "A starvation-free algorithm for achieving 100% throughput in an input-queued switch", Proc. ICCCN'96, Washington D.C., October 1996, pp. 226-231.
70. Smith Michael, John Sebastian (2005), Application Specific Integrated Circuits, Pearson Education,
71. Matthias Gries "Algorithm-Architecture Trade-offs in Network Processor Design", Doctorate dissertation at Swiss Federal Institute of Technology, Zurich, May 2001
72. Ulf Nordqvist, "Protocol Processing in Network Terminals ", Linkoping Studies in Science and Technology, Dissertation No. 865, December 2004.
73. U. Nordqvist, T. Henriksson, and Dake Liu, "CRC Generation for Protocol Processing", Norchip, Turku, Finland, 2000.
74. Ulf Nordqvist, "A Programmable Network Interface Accelerator", Licentiate Degree Thesis, Linkoping Studies in Science and Technology, Thesis No. 998, 2002.
75. Ulf Nordqvist, "On Protocol Processing", CCSSE, Norrkoping, Sweden, March 2001.
76. Persson, N., "Specification and Implementation of a Functional Page for Internet Checksum Calculation", Master's thesis, Linköping University, March 2001, No. LiTHIFM-EX-959
77. H. Obara: "Scalable Two-stage WDM Crossconnect Architecture", Electronics Letters, Jan 1996, vol. 32, no. 1, pp57-58

78. Coppo, P., et al., "Optimal Cost/Performance design of ATM Switches," Proc. Infocom 92, Florence, Italy, May 1992:446-458.
79. Douglas L. Perry, VHDL Programming by Example, 4th Edition, Tata McGraw-Hill, 2002.
80. Volnei A. Pedroni, Circuit Design with VHDL, Prentice-Hall of India, 2005.
81. M.P.Leong, O.Y.H. Cheung, K.H.Tsoi, P.H.W. Leong "A Bit serial Implementation of the International Data Encryption Algorithm," FCCM, April 2000.
82. J Raja and S Shanmugavel, "Performance Analysis of Banyan Switch Architecture", IETE Journal of research volume 49, no. 1, Jan-Feb-2003
83. Jacob J. Repanshek, "A Multi-Gigabit Network Packet Inspection and Analysis Architecture for Intrusion Detection and Prevention Utilizing Pipelining and Content-Addressable Memory", BS, University of Pittsburgh, 2003.
84. T. Saadawi, M. Ammer, EI Hakeen, "Fundamentals of Telecommunication Networks", Willey Interscience.
85. Bruce Schneier, Applied Cryptography, Second Edition Protocols, Algorithms and Source code in C John Wiley & Sons Inc., Newyork ,2001
86. E. Spitznagel, D. Taylor, and J. Turner, "Packet Classification Using Extended TCAMs," in Proceedings of IEEE International Conference on Network Protocols (ICNP), 2003
87. Shaikh, S. Z., et al., "A Comparison of the Shufflenet and Banyan Topologies for Broadband Packet Switches," Proc. Infocom 90, San Francisco, July 1990: 1260-1267.
88. William Stalling: Cryptography and Network security, Second Edition, Prentice Hall, New Jersey, 1999
89. Tanenbaum, A. S. "Computer Networks", 3rd Ed., Prentice Hall PTR, ISBN 0-13-349945-6, 1996
90. S. Stas, "Associative processing with CAMs," in Northcon/93 Conf. Record, 1993, pp. 161 –167
91. Yalamanchili Sudhakar (2002), Introductory VHDL – From Simulations to Synthesis, Pearson Education, New Delhi
92. D. E. Taylor, "Survey and Taxonomy of Packet Classification Techniques," Tech. Rep. WUCSE-2004-24, Department of Computer Science & Engineering, Washington University in Saint Louis, May 2004
93. Y. Tamir and G. L. Frazier, "Dynamically-allocated multi-queue buffers for VLSI communication switches," IEEE Transactions on Computers, vol. 41, no. 6, pp. 725-737, June 1992

94. Y. Tamir and H.C. Chi, "Symmetric crossbar arbiters for VLSI communication switches," IEEE Transactions on Parallel and Distributed Systems, vol. 4, no. 1, pp. 13-27, January 1993.
95. Henriksson, T., Eriksson, H., Nordqvist, U., Larsson-Edefors, P., Liu, D., "VLSI Implementation of CRC-32 for 10 Gigabit Ethernet", ICECS, Malta, 2001.
96. F. A. Tobagi, "Fast packet switch architectures for broadband integrated services digital networks," Proc. of the IEEE, vol. 78, January 1990, pp. 133-178
97. Mel Tsai," Network Processing Architectures: An Overview" , Presentation ,May 2000
98. J. Turner, "Design and Analysis of Switching Systems", Aug 2000
99. T. Viswanathan, "Telecommunication Switching Systems and Networks", PHI Publication, Dec-2003
100. Shah M.V., Sharma D.J, Trivedi A.I., "Modified Algorithm for High Speed Symmetric Crossbar Switch" proceeding of the international Conference on next generation networks cp25.1-cp25.5, February 2006.
101. Feghali, W., Burres, B., Wolrich, G.,Carrigan, D., "Security: Adding Protection to the Network via the Network Processor." Intel Technology Journal. <http://www.intel.com/technology/itj/2002/volume -06issue03/> (August 2002).
102. Zegura, E.W., "Architectures for ATM Switching Systems," IEEE Commun. Mag.,31,2(Feb. 1993): 28-37.
103. Haiyong Xie, Li Zhou, and Laxmi Bhuyan "Architectural analysis of Cryptographic applications for Network Processors," Workshop on Network Processors, pp 42-52 February 2002.
104. Yu-Shuan Yeh, Michael G. Hluchyj, and Anthony S. Acampora, " The knockout switch: A simple, Modular Architecture for High performance Packet Switching" , IEEE journal on selected areas in communications, vol. SAC-5,No.8. October 1987, pp. 1274-1283
105. Pankaj Gupta, "Scheduling in Input Queued Switches: A Survey". Department of Computer Science, Stanford University.
106. H. Jonathan Chao, Bin Liu, "High performance Switches and routers." <http://books.google.co.in/books>