CHAPTER 6

Development and Fabrication of CIS Thin Film Solar Cells

6. Development and Fabrication of CIS Thin Film Solar Cells

The objective of this work is to prepare and characterize copper indium dieseline (CIS) based thin film solar cell device. The two most important factors for CIS based thin film solar cell are the production cost and the efficiency. A large capital cost for the deposition equipment, in combination with a relatively long deposition time and higher thickness of CIS absorber layer leads to the high production cost for CIS based thin film solar cell. To investigate the performance of submicron CIS based thin film solar cell, numerical simulation analysis using AMPS-1D is carried out in this chapter. Layer parameters used in the simulation process are the optimized results obtained for each layer and discussed in the earlier chapters.

CIS based thin film solar cell device is fabricated and current voltage (I-V) analysis of the as- prepared device is carried out. A series of processing steps required for the fabrication of CIS thin film solar cell device are discussed in this chapter. I-V analysis of as prepared CIS solar cell device is an important tool to elucidate the performance of the solar cell. It is necessary to take I-V of solar cell as fast as possible to eliminate the effect of temperature on open circuit voltage (V_{oc}) and short circuit current (I_{sc}) as it affects efficiency of the device. For this reason the LabVIEW (Laboratory Virtual Instrument Engineering Workbench) controlled automation system is used for studying the solar cell I-V characteristics. The theory and experimental procedures used to extract the device parameters from the I-V characteristics and quantum efficiency measurement are also discussed in this chapter.

In this study, CIS solar cell having CIS thickness of 0.5 μm where as the thickness of CdS is 140nm is fabricated. Noticeable V_{oc} and I_{sc} of this device actuate us to increase the thickness of CIS in the solar cell structure. Since CIS/CdS interface is very important for the optimum performance of the device, more experiments are needed in order to understand the effect of the thickness of buffer layer on dark current voltage measurements of the device, especially when the absorber layer thickness is ~1 μm.

6.1 Simulation using Analysis for Microelectronic and Photonic Structures (AMPS-1D)

Several modeling programs have been written with a specific purpose of modeling solar cells. They have different possibilities and limitations, but the basic principles are the same. A review of different simulation methods and their advantages and disadvantages is elaborated by Burgelman [162]. One of them has been used for calculations in this work. It is Analysis of Microelectronic and Photonic Structures (AMPS-1D), as it is more stable, better plotting facilities and can run multiple simulations simultaneously. The basic concepts and material properties are discussed in the following sections. The front panel of the AMPS-1D simulation for CIS solar cell structure is shown in figure 6.1.

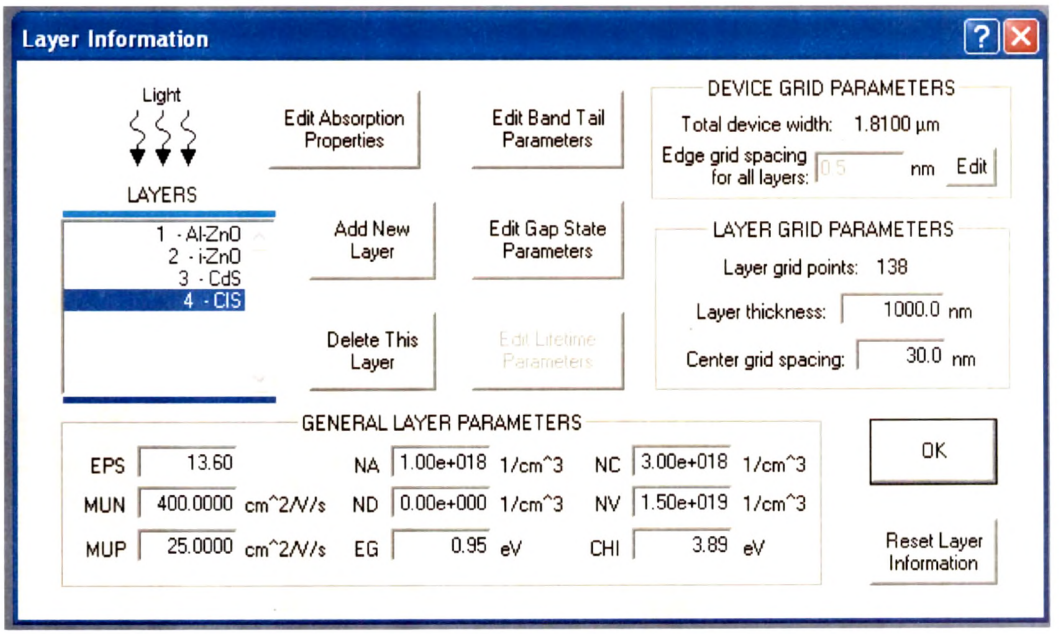


Figure: 6.1 AMPS simulation front panel contains the device and layer grid parameters, and general layer parameters.

6.1.1 Basic Concepts

AMPS-1D is used in this work; it solves numerically three coupled partial differential equations: the Poisson equation and the continuity equations for electrons and holes as a function of position 'x'. The Poisson equation connects the electric potential and the charge:

$$\frac{d}{dx}\left(-\varepsilon(x)\frac{d\psi}{dx}\right) = q\left[p(x) - n(x) + N_D^+(x) - N_A^-(x) + p_t(x) - n_t(x)\right] \qquad (6.1)$$

where, ψ is the electrostatic potential, n, p are the concentrations of free electrons and holes, n_t, p_t are the concentrations of trapped electrons and holes, N_D^+ and N_A^- are the

concentrations of ionized donors and acceptors, ε is the dielectric permittivity of semiconductor, and q is the electron charge. The continuity equation for electrons is,

$$\frac{1}{q}\left(\frac{dJ_n}{dx}\right) = -G(x) + R(x) \tag{6.2}$$

and for holes:

$$\frac{1}{q}\left(\frac{dJ_p}{dx}\right) = G(x) - R(x) \tag{6.3}$$

where J_n and J_p are the electron current and hole current, respectively. G(x) is the generation rate, and R(x) is the recombination rate, which generally involves band to band recombination and Shockley Read Hall (SRH) recombination and is nonlinear in n and p.

The illumination intensity decreases exponentially with penetration into the solar cell. The generation rate is proportional to the remaining illumination, and the exponent contains the wavelength-dependent absorption coefficient of the particular layer:

$$G(x) = -\frac{dI_x}{dx} = \alpha I(x_0)(\exp-\alpha(x-x_0)) \tag{6.4}$$

Here, I(x) is the illumination intensity at the position x, x_0 is the point at the beginning of the particular layer. The unknown variables in a solar cell simulation are the electrical potential ψ and the carrier concentrations p and n, or alternatively, the potential and the quasi-Fermi levels for electrons and holes (ψ, E_{Fn} and E_{Fp}).

6.1.2 Device Properties and Description

The device properties and their importance in numerical simulation are discussed here for understanding the impact of them on the efficiency of CIS thin film solar cell device.

6.1.2.1 Front and Back Contacts

The front and back contacts are solely defined by their work function and the reflectivity of the contact-semiconductor interface: Φ_{bo} = 0 eV, the conduction band at the Fermi level E_F at x = 0 μm (front) and Φ_{bL} = 0.9 eV (back), the conduction band above E_F at x = L (back). These numbers create an ohmic contact at the front and a negligible Schottky Barrier at the back. Strong back barriers are frequently observed in thin-film solar cells.

6.1.2.2 Surface Recombination

Interfaces between polycrystalline layers are rich in defect states, generated by lattice mismatch and impurities that cause recombination current. The parameter used to describe

this recombination current is given in terms of a surface recombination velocity [66]. All numerical calculation for this work used a surface recombination velocity of 10^7 cm/s, which corresponds approximately to the thermal velocity of the electrons.

6.1.2.3 Front and Back Surface Reflectivity

The front surface reflectivity limits current density. This parameter is set to 0.1 in order to reflect experimental data. The back reflection has only negligible influence on the performance since only few absorbable photons (close to the CIS bandgap) transverse the device and therefore gets a chance of being reflected.

6.1.2.4 Material Properties

The material parameters that define the base case are listed in table 6.1. Material properties for each layer are optimized parameters obtained in chapter 3 to 5 except the parameters like effective density of states (N_c and N_v) and electron affinity.

6.1.2.5 Environmental Conditions

The illumination is discretely defined. The number of incident photons/(cm^2.s) is entered for wavelengths between 0.38 μm and 1.24 μm, with a step size of 0.02 μm. It is unnecessary to specify the illumination spectrum beyond these limits since, CIS solar cells have only measurable efficiency in the range of 0.35-1 μm. The discrete spectrum $I_{dis}(\lambda_i)$ can be calculated from the standard AM1.5 spectrum, $I_{AM1.5}(\lambda)$, by:

$$I_{dis}(\lambda_i) = \int_{\lambda_i-0.01\mu m}^{\lambda_i+0.01\mu m} I_{AM1.5}(\lambda)\, d\lambda \qquad (6.5)$$

where $I_{AM1.5}(\lambda)$ is given in the units of photons per area × time × wavelength.

Table 6.1: Material parameters used for the simulation of CIS solar cell.

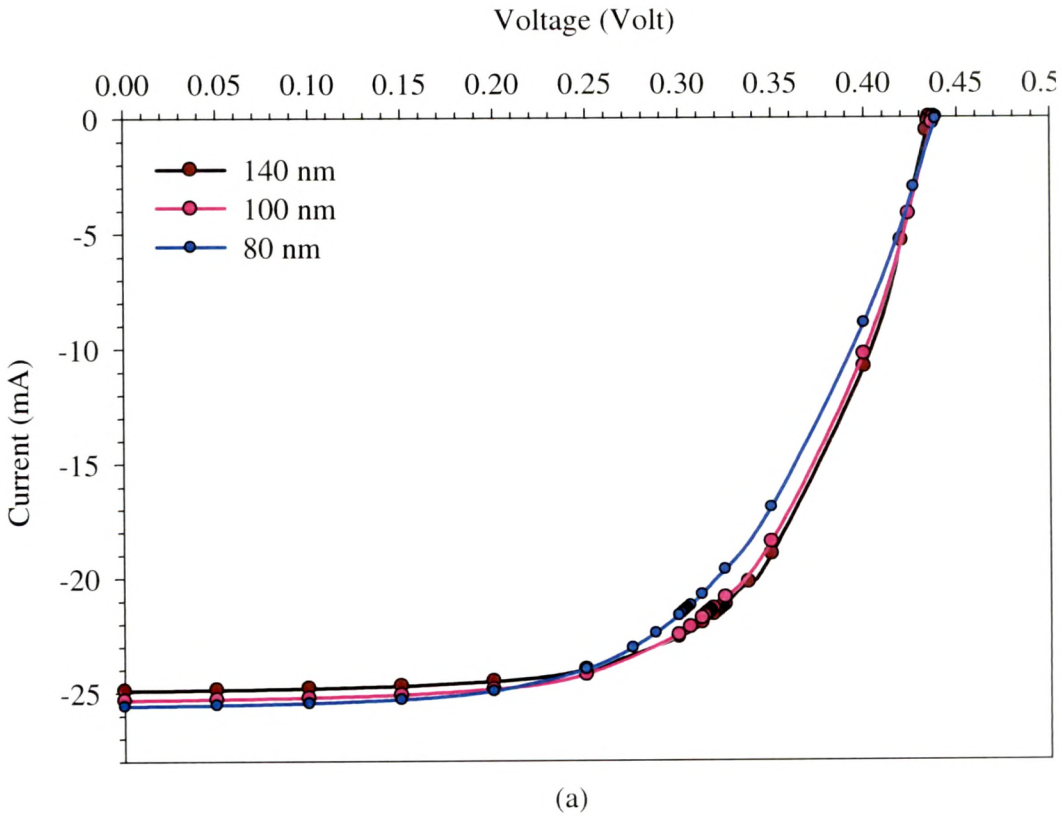
General Device Properties				
	Front Surface (x = 0.5 μm)		**Back Surface (x = 1.7 μm)**	
$\Phi_{b0/L} = E_C - E_F$ (eV)	0.0 eV		0.9 eV	
Surface recombination electrons (cm/s)	10^7		10^7	
Surface recombination holes (cm/s)	10^7		10^7	
Reflectivity	0.1		0.8	
Layer Properties				
	AZO	**i-ZnO**	**CdS**	**CIS**
Thickness (nm)	600	50	80-140	1000
Dielectric constant	9.0	9.0	10.0	13.6
Electron mobility (cm^2/Vs)	50	50	1-20	50
Hole mobility (cm^2/Vs)	5	5	25	5
Carrier density n or p ($1/cm^3$)	$1.7E+10^{19}$	5E+16	10^{17}	10^{18}
Bandgap (eV)	3.3	3.3	2.4	0.95
Effective density N_C ($1/cm^3$)	1.00e+19	1.00e+19	1.00e+19	3.00E+18
Effective density N_V ($1/cm^3$)	1.00e+19	1.00e+19	1.60e+19	1.5E+19
Electron affinity (eV)	3.9	3.9	3.8	4.1

6.1.2.6 Modeling Setting

The AMPS software can operate in two distinct modes: the density of state (DOS) mode or the lifetime mode. A description of both modes can be found in the AMPS manual ; a comparative discussion is given in A.L. Fahrenbruch's work on CdTe solar cells [163]. In essence, the lifetime mode accepts inputs in the form of carrier lifetimes, which are assumed constant, independent of light and voltage bias, and does not address the underlying recombination processes. The DOS mode allows the definition of multiple defect states, using densities, energy distributions, and capture cross-sections. All modeling done for this work used the DOS mode. The grid spacing is selected to be denser in the thinner top layers of the device, where more rapid changes are to be expected in the band structure. Selected biases are entered as necessary.

6.2 Analysis of Simulated Current-Voltage Measurement (I-V) Results for Various Thicknesses of CdS Buffer Layer

CIS based thin film solar cell have a complex multilayer structure, consisting of a thin buffer layer (CdS or an alternative) and a double TCO layer (e.g. nominally undoped ZnO followed by Al doped ZnO). Figure 6.2(a) shows the simulated I-V characteristics of the CIS solar cell structure having a CIS thickness of 1 μm with different thickness of buffer layer obtained using AMPS-1D. Figure 6.2 (b) shows the variation in the V_{oc} and FF including η as a function of buffer layer thickness. It is seen that open circuit voltage (V_{oc}) decrease with increasing CdS buffer layer thickness as shown in figure 6.2 (b). This is because a thicker buffer layer will result in higher photon loss. When the thickness of the buffer layer is increased, more photons which carry the energy are absorbed by this layer. Therefore it would lead to a decrease in the photons which have reached the absorber layer. Fill factor increases slightly as the buffer layer thickness increases. It can be due to less discontinuity at the absorber and buffer layer interface. As the thickness of the layer increases from 80 nm to 140nm, the conversion efficiency increases from 6 % to 7 %. Solar cell with 140 nm of CdS buffer layer recorded the highest efficiency for the whole CdS/CIS cases. This is due to increase in fill factor. It is found that the optimum buffer thickness would be 140 nm.



(a)

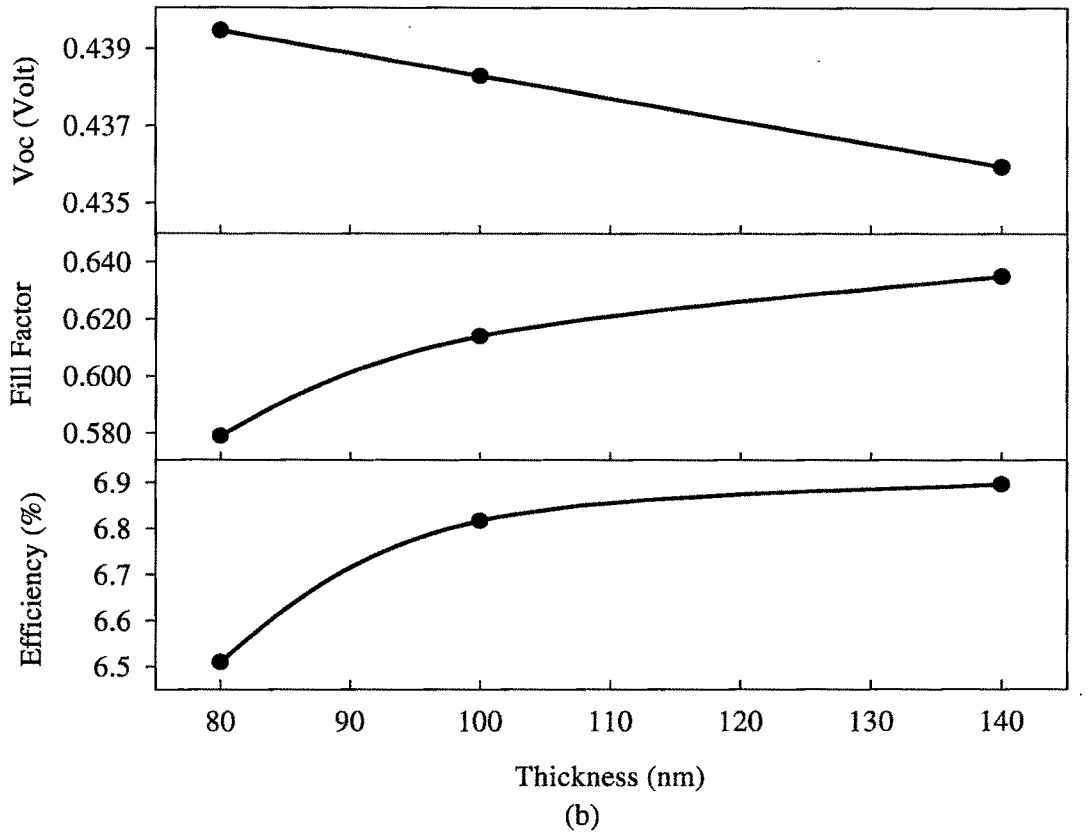


Figure 6.2 (a) Illuminated I-V curves with different buffer layer thickness, (b) Variation of V_{oc}, FF and efficiency with buffer layer thickness.

6.3 CIS Thin Film Solar Cell Device Fabrication Process

6.3.1 Substrate Preparation and Molybdenum (Mo) Back Contact Deposition

All films considered in this study are deposited on microscope glass slides made of soda lime glass known as substrate. The quality of the substrate, prior to deposition of device quality thin films, is a crucial factor, which influences the material properties of the deposited thin films. Surface defects such as scratches and dust on the substrate have an adverse effect on the structural properties of the thin films. In order to obtain a high degree of chemical cleanliness of the substrate, the following procedure is followed:

- The substrate is ultrasonically cleaned using the soap solution prepared in warm distilled water.
- Substrate is then organically cleaned, in turn, under vapors of methanol, acetone, and trichloroethylene, respectively, to remove contaminants on the glass substrate.
- A number of glass substrates are cleaned and kept under clean conditions.

For deposition of Mo thin films on organically cleaned glass substrate, the vacuum coating unit is evacuated to a base pressure of around 10^{-5} Torr. The Ar gas is introduced in the vacuum chamber using the needle valve and rotameter arrangement. The chamber pressure is maintained at the desire level, by partially closing the baffle valve and adjusting the flow of Ar gas using needle valve. Low resistive (~1 Ω/□ sheet resistance), well adherent Mo thin films are obtained at room temperature by controlling the deposition parameters of Mo thin film as listed in Table 6.2.

Table 6.2: The typical deposition parameters of Molybdenum thin films onto glass.

Deposition parameters	Optimum value
Target to substrate distance	90 mm
RF power	100 W
Working pressure	1 mTorr
Substrate rotation	~ 40 RPM
Sputter gas	Argon
Rate of deposition	3-3.2 Å/s
Thickness	1000 nm

6.3.2 CIS, CdS and ZnO Thin Film Deposition

CIS thin film solar cell device has complex structure comprising of various layers as shown in figure 1.3. Each layer is fabricated using different deposition technique viz. ZnO front contact via, RF magnetron sputtering; CIS absorber using Flash evaporation technique; and CdS using thermal evaporation. Figure 6.3 illustrates the whole fabrication process of CIS thin film solar cell. In the first stage molybdenum thin film is deposited on 5 x 5 cm^2 ultra cleaned glass substrates. using optimized deposition parameters depicted in Table 2.1 The as-prepared molybdenum coated glass is carefully cut into squares of 2.5 x 2.5 cm^2 One of the squares is used for deposition of various layers i.e. CIS, CdS, i-ZnO, AZO. To fabricate each layer specially designed masks are used to avoid shunting between the layers. The methods used to deposit various layers and optimized deposition parameters are discussed in chapter 3-5.

6.3.3 Aluminum Grid Deposition

Thermal evaporation technique is used to deposit 1μm aluminum (Al) thin film in the finger type pattern, through a metal mask onto the ZnO:Al window layer. The mask is designed to cover less than 10 % of the total active cell area. Evaporation of Al is carried out at 10^{-5} Torr base pressure at a deposition rate of 0.4 nm/sec. The rate of deposition and thickness of Al film is monitored using quartz crystal.

6.4 I-V Characterization of CIS Thin Film Solar Cell Device

6.4.1 Theory of I-V Analysis

The I-V characteristic of the Mo/CIS/CdS hetrojunction is obtained by applying voltage across the junction and measuring the resulting current. A positive voltage is applied to the Molybdenum back contact and a negative voltage is applied to small Indium dot on CdS layer. The I-V characteristic is measured for Mo/CIS/CdS heterostructures. The n-type CdS and p-type CIS form a rectifying junction, whose behavior is similar to that of an abrupt p-n junction. The behavior of an abrupt p-n junction is governed by the ideal diode equation given below,

$$I = I_0\left(\exp\left(\frac{qV}{nkT}\right)-1\right) \tag{6.6}$$

where,

I_0 – Reverse saturation current,

q – Charge of an electron

V – Voltage applied to the abrupt p-n junction,

n – Diode ideality factor,

k – Boltzman constant = 1.38×10^{-23} J/k

T – Absolute temperature in degree Kelvin.

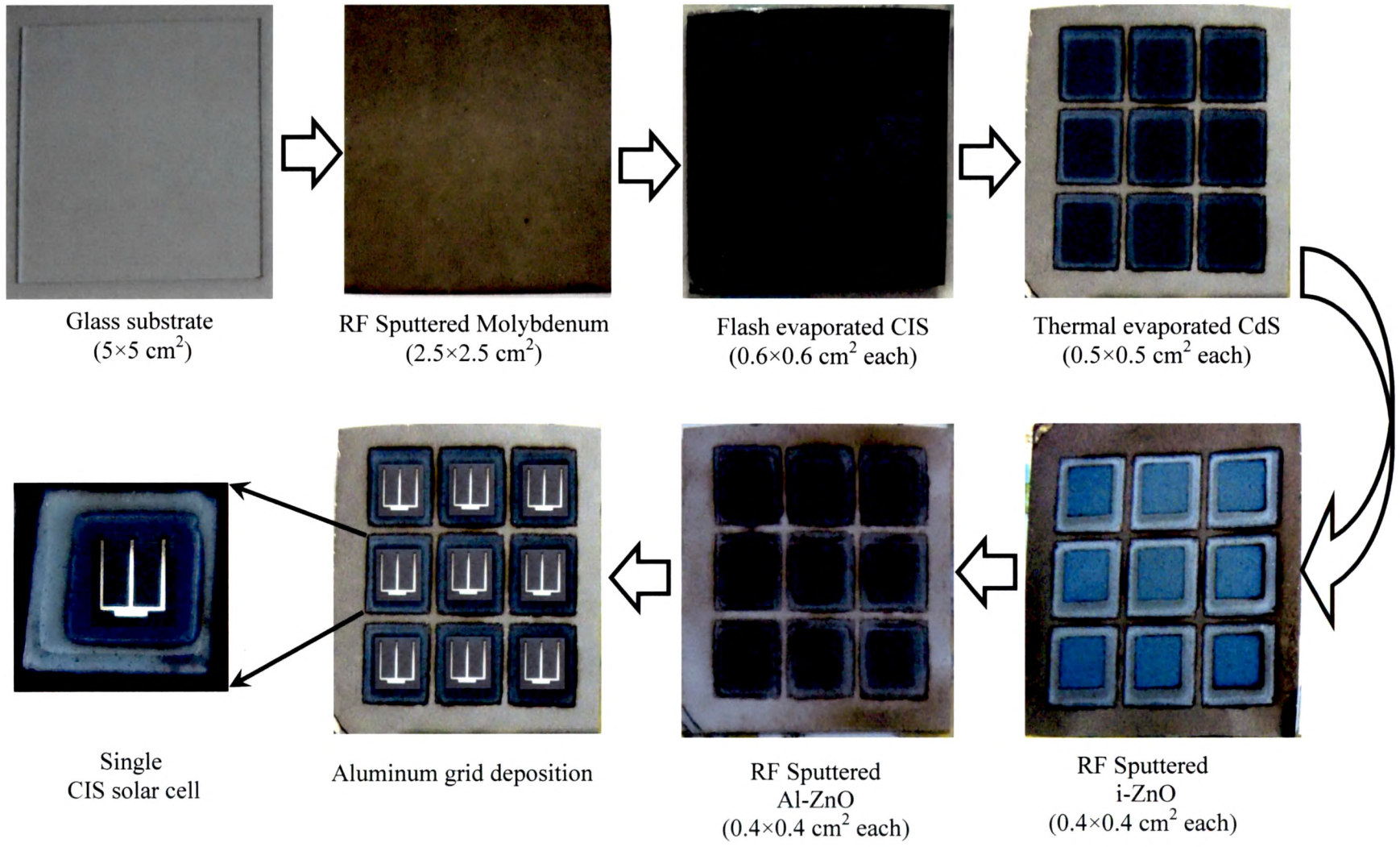


Figure 6.3 Device fabrication process steps

From the ideal diode equation it can be deduced that,

- The drift and diffusion current components cancel each other when there is no applied bias (V = 0), resulting in no net current flow across the junction.
- When the applied voltage is positive (V > 0 i.e. forward bias), the barrier for majority carrier diffusion is lowered resulting in an exponential increase in current through the junction. The drift current remains unaltered.
- When the applied voltage is negative (V < 0 i.e. reverse bias), the barrier for majority carrier diffusion is increased resulting in a negligible diffusion current through the junction, while the drift current remains unchanged. Most practical diodes have current transport mechanisms which deviate from that described by the ideal diode equation. These non-ideal currents arise as a result of generation and recombination of carriers in the depletion region, tunneling of carriers between states in the bandgap, and high-injection conditions which may arise even at a relatively small forward bias. The ideal diode equation has to be modified accordingly for these cases.

The Current-Voltage analysis of a curve involves the determination of diode parameters namely, diode ideality factor 'n', reverse saturation current density 'I_0' and the series resistance associated with the device. The sections below explain the estimation of these parameters from a given I-V curve.

6.4.1.1 Determination of Series Resistance (R_s)

The J-V characteristics of a hetrojunction diode become linear at high voltages and high currents due to the series resistance associated with it. The series resistance in the device arises due to the resistance offered by the quasi-neutral region in the p and n type materials forming the hetrojunction and the resistance of the ohmic contacts to the device. In such a case, the voltage drop across the device is not just the drop across the p-n junction, but also includes the drop due to the series resistance, R_s. In order to get the value of the voltage drop across the diode junction, the drop due to the series resistance has to be subtracted from the measured voltage drop. This makes sure that the I-V characteristic is corrected for series resistance and the current component only due to the diode behavior is extracted. Equation 6.6 modified for series resistance, R_s would be,

$$I = I_0\left[\exp\left(\frac{q(V\text{-}IR_s)}{nkT}\right) - 1\right] \tag{6.7}$$

where, R_s is the series resistance and the actual drop across the junction would be ($V - IR_s$). The series resistance can be mathematically determined from the I-V characteristic as explained below. Differentiating equation 6.7 with respect to I results in,

$$1 = I_0\frac{q}{nkT}\left(\frac{dV}{dI} - R_s\right)\exp\left[\frac{q(V\text{-}IR_s)}{nkT}\right] \tag{6.8}$$

Now,

$$\frac{dV}{dI} = \frac{nkT}{qI_0}\exp\left[\frac{-q}{nkT}(V\text{-}IR_s)\right] + R_s \tag{6.9}$$

Ignoring the reverse saturation current density, J_0, equation 6.9 can be written as,

$$\frac{dV}{dI} = \frac{nkT}{qI} + R_s \tag{6.10}$$

when the junction is biased at a high voltage, the current through it would also be high. Thus, the first term on the right side of equation 6.10 can be neglected. Hence at a higher bias voltage (and hence a higher I), the series resistance can be approximated as the slope of the I-V curve.

6.4.1.2 Determination of Ideality Factor and Reverse Saturation Current

This section explains the mathematical determination of ideality factor and the reverse saturation current density from the I-V characteristic. A plot of ln(I) Vs. V is needed in order to estimate n and I_0. Obtaining the natural logarithm of equation 6.7,

$$\ln(I) = \ln(I_0) + \frac{qV}{nkT} \tag{6.11}$$

This represents the equation of a straight line, with q/nkT as its slope and (V, ln(I)) as the variables. Once the slope of the curve is known, the ideality factor can be easily computed, as the values of q, k and T are known already. The y-intercept of the line would give the value of $\ln(I_0)$, from which the reverse saturation current density can be calculated. The value of n gives a fair idea of the ideality of the device. For an ideal diode the value of n would be 1. In the case of practical diodes, the value of n deviates from 1 due to a various reasons such as, generation-recombination processes in the depletion region, high-injection conditions and tunneling of carriers between states in the bandgap.

The block diagram of experimental set-up used to measure solar cell I-V characteristics is shown in figure 6.4. The Metal Halide bulb (150 W) is used as an irradiation light source. The Keithley 2420C programmable source meter is used in a four

wire configuration to measure I-V characteristics since it can make accurate I-V measurements automatically by simultaneously measuring the voltage and current. The main reason for using this instrument is its ability to perform I-V measurements accurately in the range of micro-ampere (μA) [164].

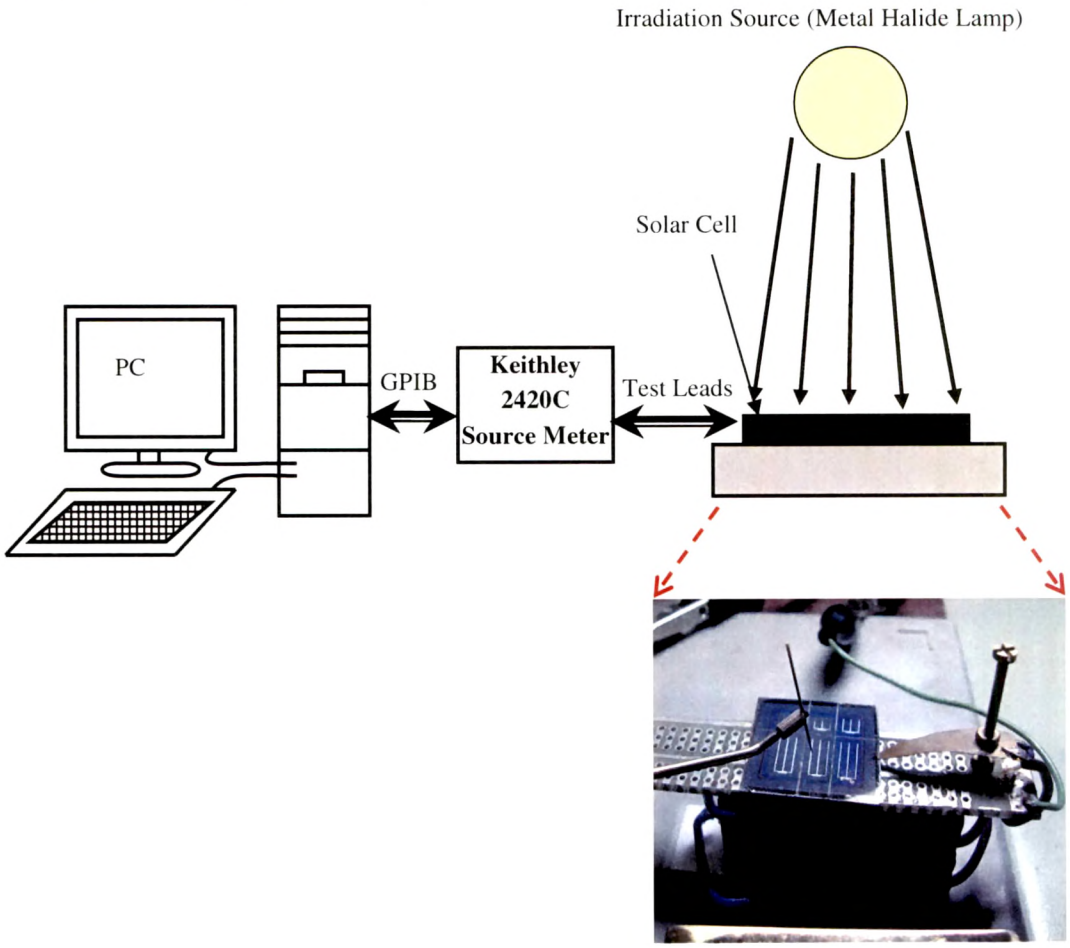


Figure 6.4: The block diagram of experimental set-up used to measure solar cell I-V characteristics.

Measurement results are sent via a GPIB interface to a computer, allowing for data acquisition and remote control for further processing. National Instrument's LabVIEW programming language is used as system software to obtain dark and illuminated I-V data [165]. The basic idea of using the LabVIEW program for the solar cell I-V characteristics is to minimize the direct irradiation time of metal halide bulb to the solar cell. The developed LabVIEW program for measuring the I-V characteristics of the solar cell has two parts, 1) dark I-V measurements and 2) illuminated I-V measurements.

By selecting the dark I-V tab form the front panel of the LabVIEW program, one can start the dark I-V measurement program. Before running the program the solar cell should be placed in the dark environment. According to the value of source voltage range, steps and delay, the source meter source the voltage and measure the current. Simultaneous plotting of I-V curve is possible using LabVIEW. By selecting the data save option one can save the data (in .xls format) as well as curves (in .bmp format). The front panel of the LabVIEW program for the Dark I-V measurements is shown in figure 6.5. The ideality factor, (n), and saturation current, (I_0) of the solar cell is automatically calculated from the plot.

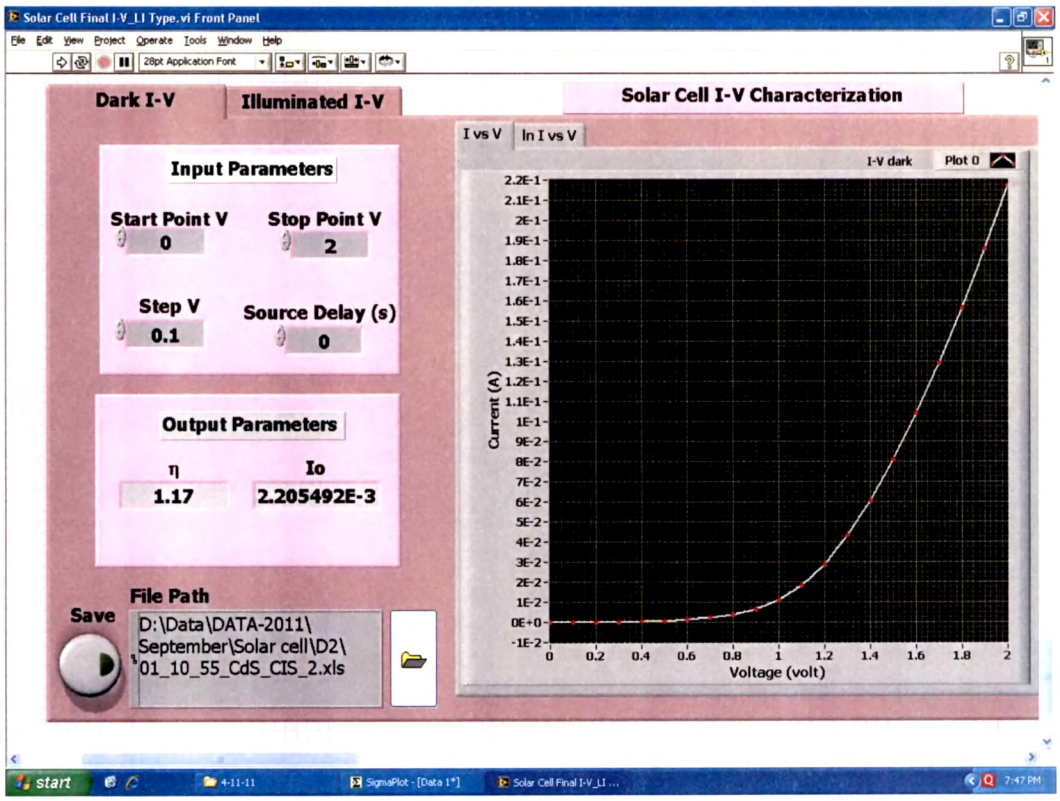


Figure 6.5: Front panel of LabVIEW program for dark I-V measurements of commercial solar cell.

The illuminated I-V measurement for the solar cell is carried out by keeping it under the solar irradiation source. For that we have used metal halide (150 W) as a light source. After adjusting the input power to the solar cell, viz AM. 1.5 or AM 1, area of solar cell and setting the parameters same as in dark I-V and running the program, the graph of illuminated I-V is plotted. Figure 6.6 shows the front panel of the illuminated I-V measurement of commercial solar cell.

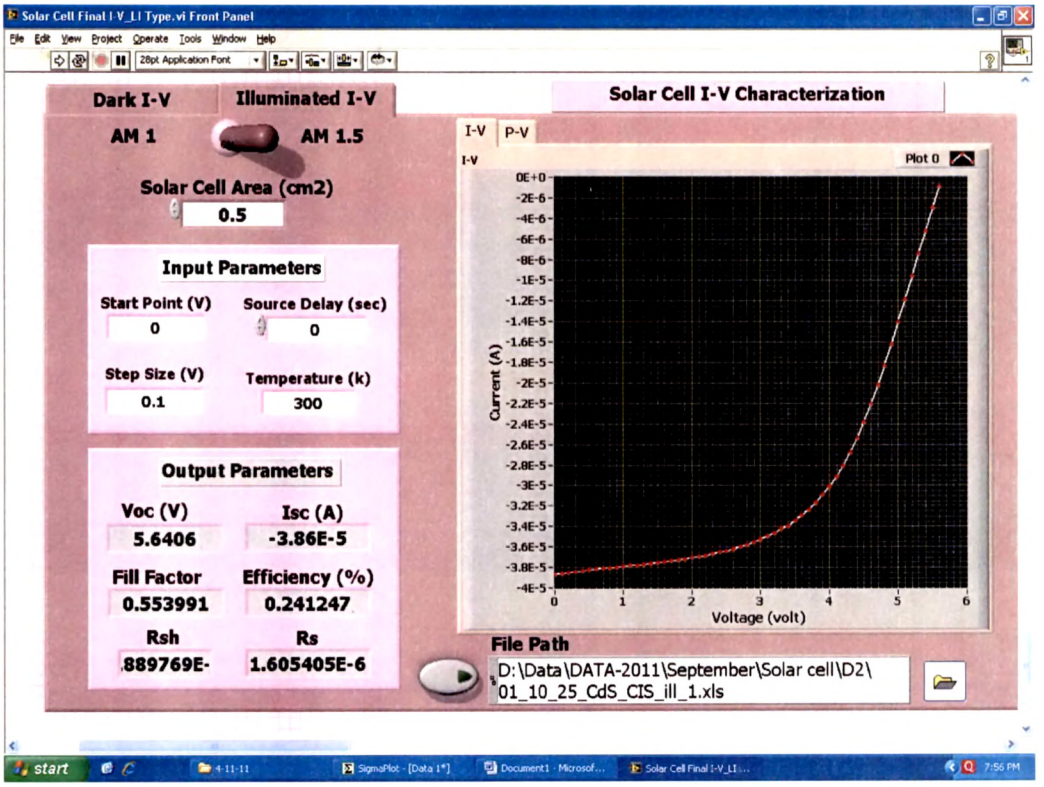


Figure 6.6: The front panel of the LabVIEW program for the illuminated I-V measurements of commercial solar cell.

6.5 Quantum Efficiency Measurement

Quantum-efficiency measurements (QE) quantify the spectral response of a device. The photocurrent response to a monochromatic probe beam is measured, with QE defined as,

$$QE(\lambda) = \frac{\text{No.of electrons collected}}{\text{No.of incident photons}} \tag{6.12}$$

The current response of the reference device (silicon detector) is measured ($I_{ref}(\lambda)$), and the current response of the device-under-test is measured ($I_{test}(\lambda)$). The QE of the test device is obtained from,

$$QE_{test}(\lambda) = \frac{I_{test}(\lambda)}{I_{ref}(\lambda)} \tag{6.13}$$

A schematic diagram for the QE measurement used in this work is shown in figure 6.7. A tungsten halogen lamp is used as the light source at the input slit of the monochromator. The monochromator (CM110) is a dual-grating monochromator manufactured by Stanford research. The spectral width of the probe-beam at the output of the monochromator is 1 nm. A chopper controller controls an optical chopper. The beam is then collimated and focused into a 2×2 mm spot on the solar cell device. The quantum-

efficiency measurement setup is computer controlled using LabVIEW (Version 8.2) software. QE data is taken in the range 400–1600 nm at 5 nm intervals at room temperature.

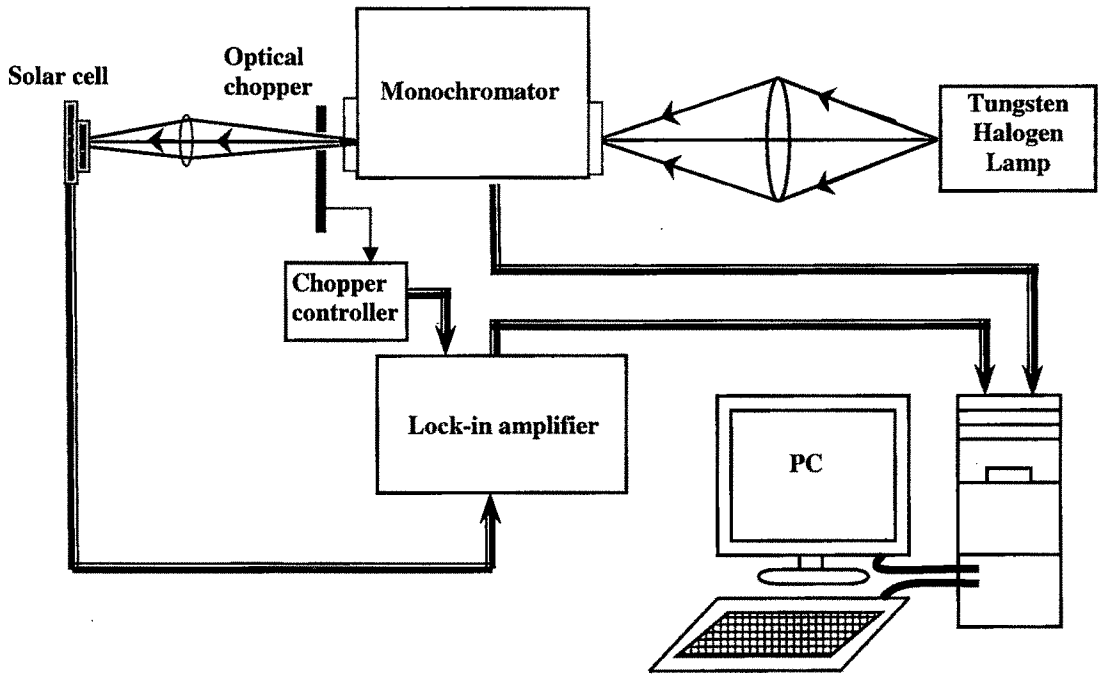


Figure 6.7: A Schematic diagram for the QE measurement.

The quantum-efficiency measurement setup is computer controlled using LabVIEW (Version 8.2) software. QE data is taken in the range 400-1600 nm at 5 nm intervals at room temperature. Figure 6.8 shows front panel of QE measurement.

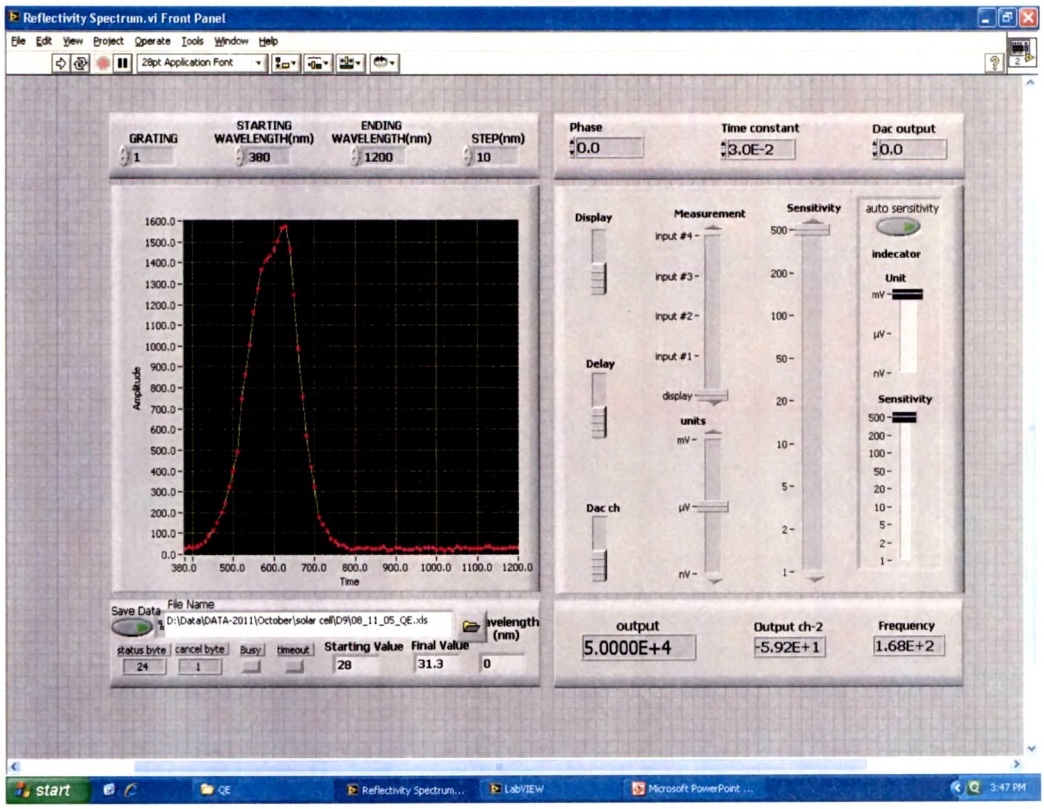


Figure 6.8: The front panel of the LabVIEW program for the QE measurements of commercial solar cell.

6.6 Dark and Illuminated I-V Analysis of Fabricated CIS Devices

The objective of this study is to analyze electrical characteristics of fabricated CIS solar cell. During dark I-V measurements, the photogenerated current is eliminated by placing the sample (solar cell) in a dark enclosure. In order to perform dark I-V measurements, a dark I-V system consists of a voltage source controlled by computer, and a sample holder. Figures 6.4 shows block diagram of experimental set up used to perform I-V measurements. The sample is forward biased to a pre-set voltage, and the resulting current is measured, obtaining the I-V relationship. I-V data generated is analyzed and the necessary device parameters are determined.

6.6.1 Results of CIS Solar Cell with CIS Thickness of 0.5μm

In this study fabricated CIS solar cell having CIS thickness of 0.5 μm and CdS buffer layer thickness of 140 nm. Figure 6.8 shows dark I-V curve of the attempted solar cell. It is evident from figure 6.9 that the dark I-V measurements do not reveal all regions that describe the dark I-V profile. Ideality factor evaluated from the plot is very high (~14.8).

The deviation of ideality factor from 1 indicates recombination of charge carriers at the interface. The illuminated I-V characteristic of fabricated CIS solar cell device having CIS thickness of 0.5 μm can be obtained by illuminating the device using Metal Halide Bulb. The illuminated I-V plot of the fabricated device is shown in the figure 6.10. V_{oc} and I_{sc} obtained from the illuminated I-V curve is ~70 mV and ~1 mA respectively. The V_{oc} and I_{sc} of this device having CIS layer thickness of 0.5 μm is significantly lower than the standard values.

This is due to the very narrow space-charge region formation for the lower thickness of CIS absorber [166]. As the thickness is reduced by a factor of 4 compared to the standard, there could be significant back contact recombination. The device may become electrically shunted when the thickness is reduced to 0.5 μm. I-V curves of this device show significant collection problems also.

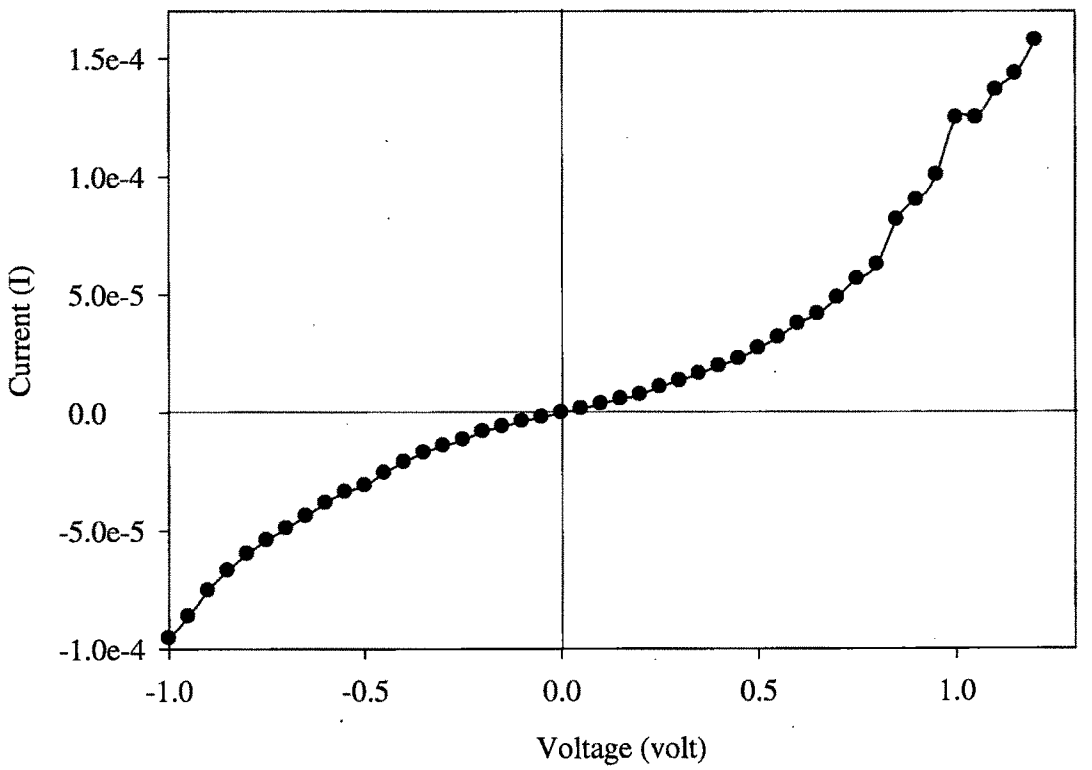


Figure 6.9: Dark I V plot of CIS (thickness 0.5 μm) solar cell having buffer layer thickness of 140 nm.

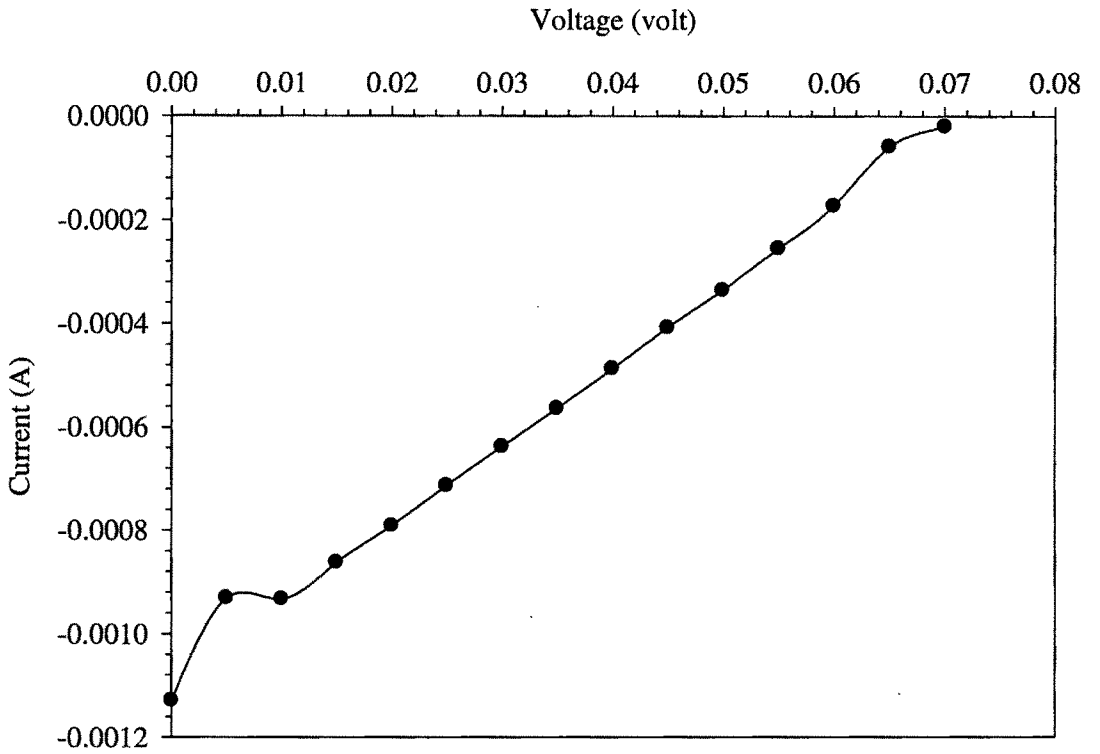


Figure 6.10: Illuminated I-V plot of CIS (thickness 0.5 μm) cell having CdS thickness of 140 nm.

The lower I_{sc} may be due to the increase in bandgap of the absorber and unfavorable interface effects. Hence, it is concluded that thickness of 0.5μm affects the performance of the device to a large extent. To understand the reason for the loss in currents and voltage attempts are made to fabricate devices with CIS layer near to 1 μm. As CIS/CdS interface is important for the optimum performance of the devices more experiments have been carried out to understand the effect of the thickness of buffer layer on dark I-V measurements, especially when the absorber layer thickness is ~1 μm

6.6.2 Dark I-V Results of Mo/CIS/CdS Structure with CIS Thickness of 1 μm and Different Thickness of CdS

This section presents the results of dark I-V data obtained for CIS solar cells having varying CdS buffer layer thickness. In this study, dark I-V measurements are performed for both forward and reverse bias. Under forward bias ($V > 0$), the dark I-V measurement profiles indicate the effect of shunt resistances Reverse biasing ($V < 0$), however, allows the effect of reverse saturation current of a solar cell.

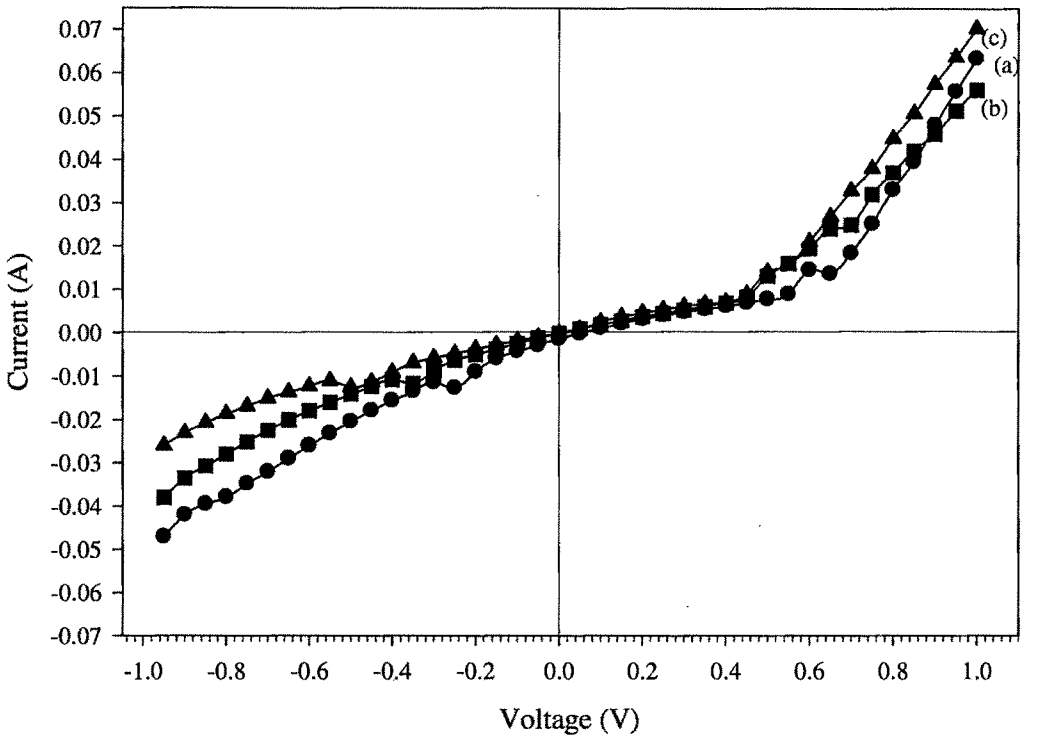


Figure 6.11: Dark I-V curves of Mo/CIS/CdS layer with different thickness of CdS layer, (a) 80 nm, (b) 100 nm, (c) 140 nm.

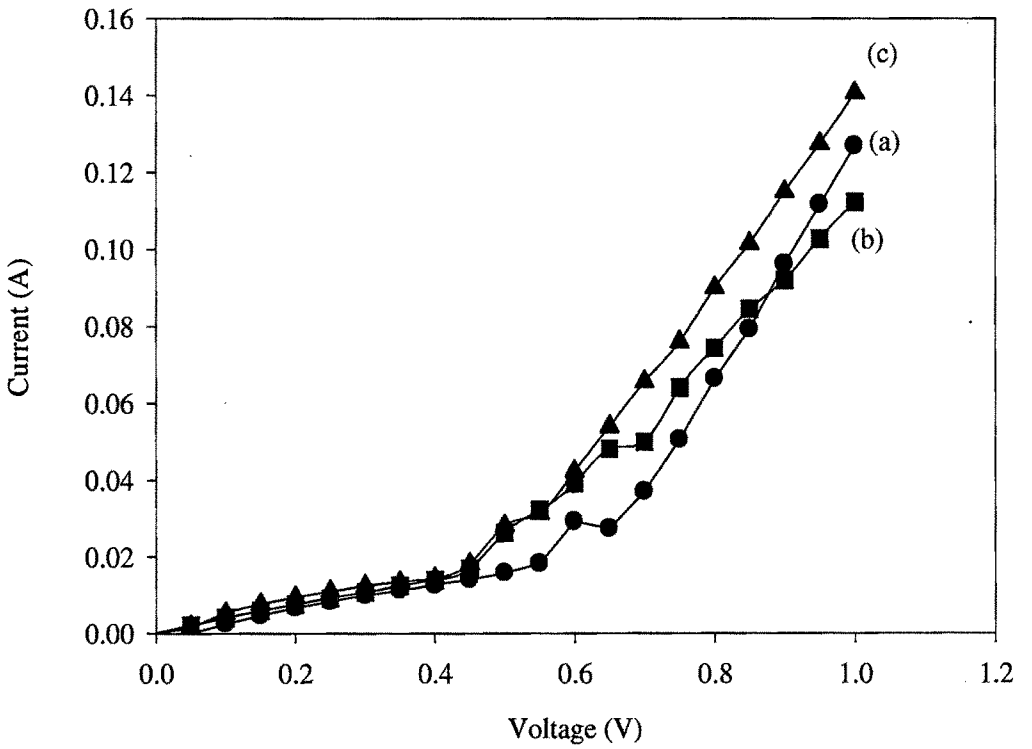


Figure 6.12: Forward dark I –V curves of CIS/CdS layer with different thickness of CdS layer, (a) 80 nm, (b) 100 nm, (c) 140 nm.

Each Mo/CIS/CdS structure has area of 0.25 cm^2. Dark I-V characteristic for Mo/CIS/CdS layer with varying thickness of CdS buffer layer is shown in the figure 6.11. During dark I-V measurements, forward biasing is achieved by making contacts on the areas. Figure 6.12 shows the forward dark I-V curve of Mo/CIS/CdS structure used for the measurement of ideality factor and reverse saturation current. Table 6.2 lists parameters obtained from the I-V measurements of Mo/CIS/CdS structure.

Table 6.2 Parameters obtained using the measured dark I-V data.

Thickness of CdS buffer layer (nm)	Reverse saturation Current I_0 (mA)	Ideality Factor n	Series resistance R_s (ohm)
800	13.41	4.92	8.96
1000	12.97	4.82	8.88
1400	12.84	4.76	7.28

It is seen that the cells have different ideality factor values because of the shape of the I-V curve. The saturation current arises when the electron-hole recombination changes in a p-n junction. During the injection process, recombination current or diode current is very much dependant on the number of injected carriers. Saturation current J_0 increases with an increase in the injection process.

Conclusions

This chapter has presented the capabilities of computer simulation for photodiode analysis to investigate performance of CIS based thin film solar cells with submicron absorber layer thickness. The selection of all input parameters for a reasonable baseline is presented. Reasonable value of efficiency at near 1 micron absorber layer thickness motivated us to fabricate CIS based thin film solar cell device.

Experimental results for the two different thicknesses of CIS layer viz 0.5 μm and 1 μm are investigated. The V_{oc} and I_{sc} of the device having CIS layer thickness of 0.5 μm is significantly lower than the standard values. The I-V curves of these devices also show significant collection problems. The I_{sc} of the device is also very less. Hence it is concluded that thickness of 0.5 μm has a detrimental effect on the performance of the devices to a large extent. Results of dark I-V measurements of Mo/CIS/CdS structure with CIS thickness of 1 μm and varying CdS thicknesses suggests that ideality factor decreases with increase of buffer layer thickness.