CHAPTER FOUR

DESIGN OF DIGITAL CONTROLS AND EMI-EMC CONSIDERATIONS FOR STATCON INSTALLATIONS IN AUTOMOBILE PLANT AND RAILWAYS SUBSTATION

4.1 INTRODUCTION

With the proliferation of the electronics controls in the power systems applications, Design integration of self commutated devices such as power MOSFETs and IGBTs (Isolated Gate Bipolar Transistor) with Microprocessors/ Micro-controllers/ Digital Signal Processors has become inevitable. However, beyond the functional simulation and known topologies which establishes the concept, to make practical design, there are always additional efforts which make the product design and development experience very special. Such an experience varies with the applications and also with the engineers. However, there are always some experiences which form the bottom line and if shared would be of good help to the other design engineers. This chapter introduces initially to the digital controls design for Power Electronics (PE) application and then highlights the installation experience of a low KVA IGBT based converter-STATCON for Reactive Power Compensation in automobile plant and railway substation. It is then followed with vital considerations for converter component layout, grounding, earthing, Printed Circuit Board (PCB) design care and many other relevant issues to achieve a reliable operations against the Electro-Magnetic Interference (EMI) ambient within a cubicle from both hardware and software perspective.

4.2 DESIGN OF DIGITAL CONTROLS

A multitude of factors influence digital core selection for PE systems [40,141]. The most important selection criterion typically from PE application requirements, is on-chip integration, performance, energy efficiency and cost. Software development tools and availability of software modules/libraries/algorithms also influence selection. Other than this vendor's support for the new devices also becomes an important aspect in developing country like ours.

In the market there are varieties of microcontrollers and microprocessors/digital signal processors from various vendors. The currently available vendors and the variety of processors they offer are listed in the earlier chapter 2. A detailed update of the DSP as on date is also covered in the reference [147].

There are some important design considerations that can facilitate choice to identify the most suitable one from sea of different processors/DSPs available. Some important considerations are covered below.

From technical context, on-chip integration, implying the digital core having the right kinds of peripherals, memory and Analog-Digital input output interface integrated within the chip remains as key. The digital core can also offer glue less interface with external peripherals, and thereby improve performance, reduce energy consumption, increase reliability and help lower system costs. From Performance view point, processing speed requirements of typical PE control applications are moderate from about 40 MHz to 150 MHz. Some other aspects which needs to be taken care for prototype development is programmability and reprogrammability for firmware. Consideration to have digital core with internal flash or EEPROM program memory (which can be erased and reprogrammed) a substantial number of times also is desirable. There are also digital core that can be used with external memory, one-time programmable chips (potentially usable after one have a working design, but losing their price advantage anyway), and mask-programmed chips (not preferred option for PE products).

From on chip peripherals context, on the output side, it is desirable to have provision for on chip Pulse Width Modulated (PWM) generation with possibility of dead band features including options for selecting different carrier frequency for modulating signal comparison so as to have direct interface with one or more, parallel or independent power devices in full bridge or half bridge configurations. Current sourcing/sinking capacity also can be important if power switches are controlled through them in buck-boost converters or LEDs or transistors are driven directly from them. On the input side, it is equally important to have Analog to Digital (A to D) converter, which can facilitate the A to D conversion for number of channels within a given power cycle. Typically, for PE application need is for 8 to 12 channels (3 for input voltage, 3 for input current, 3 for output load current feedback and one minimum for DC bus feedback). Facilities of direct triggered scheduled Analog to Digital conversion; with conversion time less than couple of microseconds is desirable to achieve sub cycle real time computation needs. Also high speed input-outputs and/or controllable interrupts are desirable for facilitating synchronization and emergency shutdown in cause faults. From application criticality, availability of watchdog timers for graceful recovery also holds an important dimension. Additional features like UARTs, SPI or

I2C, Ethernet, CAN, USB or even multiple serial ports can also enhance further application usage.

Physical packaging of the chip also is an important aspect, both from prototype development and manufacturing due to limitation on probing on the processor chip and difficulty in having the new generation processors sockets mountable for future replacements.

Particularly from PE application of power quality improvement most critical parameters thus are ADC & PWM. Taking this as backdrop, a typical growth of digital core technology solution for power converter control requirements can be best understood from the figures presented below considering the development from traditional solution to the most modern solution with the integration features which are available over last four decades.

4.2.1 SOLUTION WITH 8085/8086 BASED CONTROLLER

As shown all the blocks needs to be implemented through discrete peripheral components to achieve the functionality when implemented through processors from 1970s like 8085/8086.

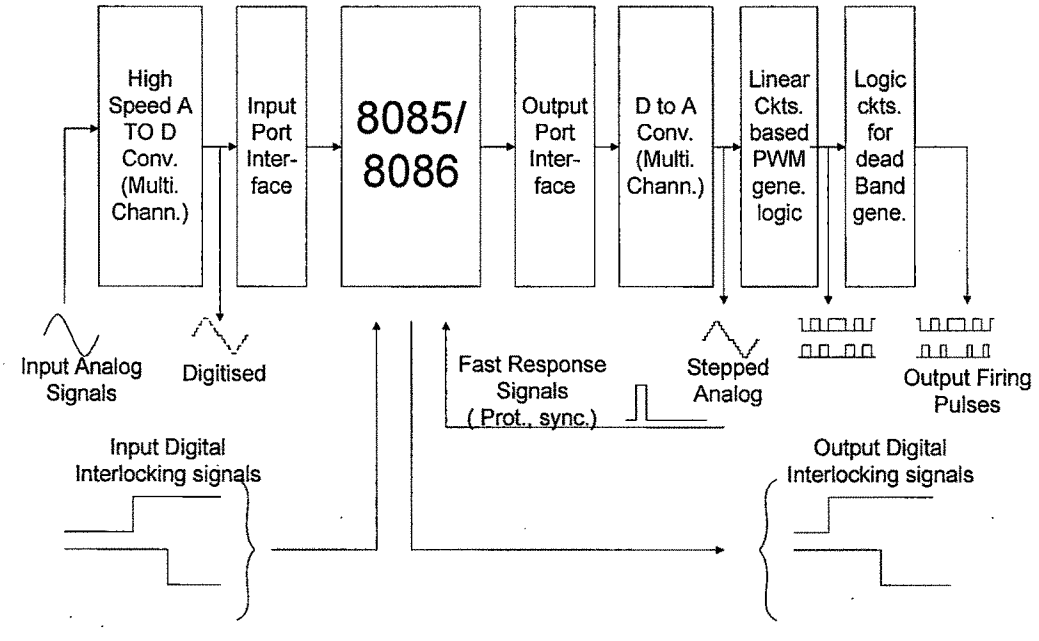


Fig. 4.1 Solution with 8085/8086 based controller

4.2.2 SOLUTION WITH 8051 BASED CONTROLLER

As shown the blocks in blue can be integrated and there are some blocks which are shown in red, which based on MCS 51 variants can also be integrated within the microcontroller. Even the base 8 bit architecture limitation of 8051 can be overcome with its 16 bit variants which are now available.

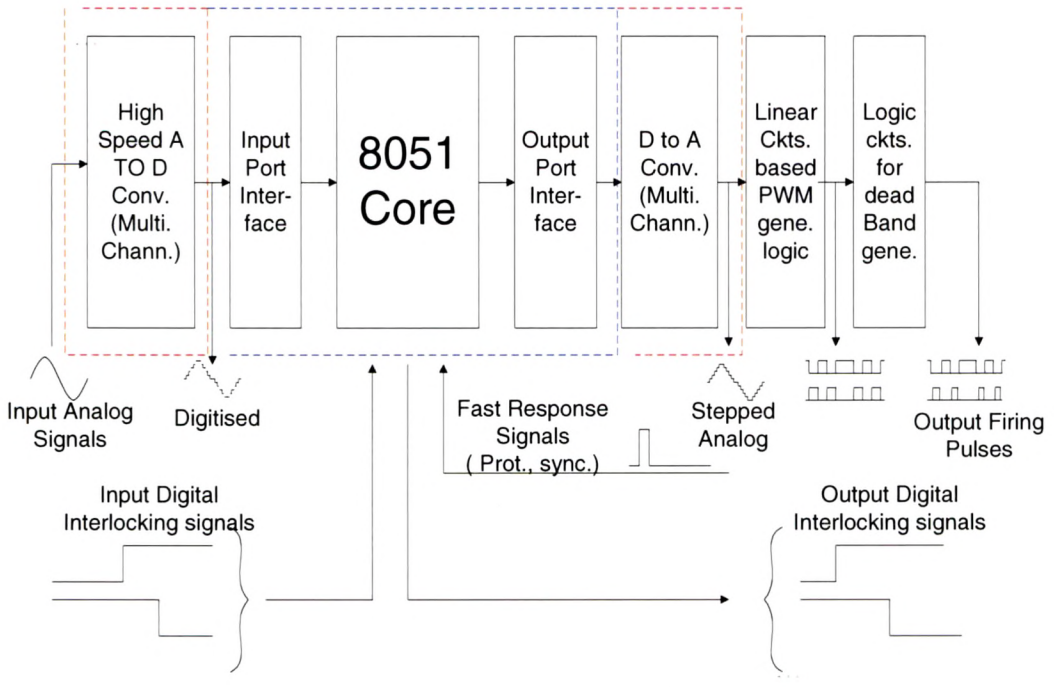


Fig. 4.2 Solution with 8051 based controller

4.2.3 SOLUTION WITH MCS 96 BASED CONTROLLER

This solution facilitates most of the blocks getting integrated on chip as shown in blue.

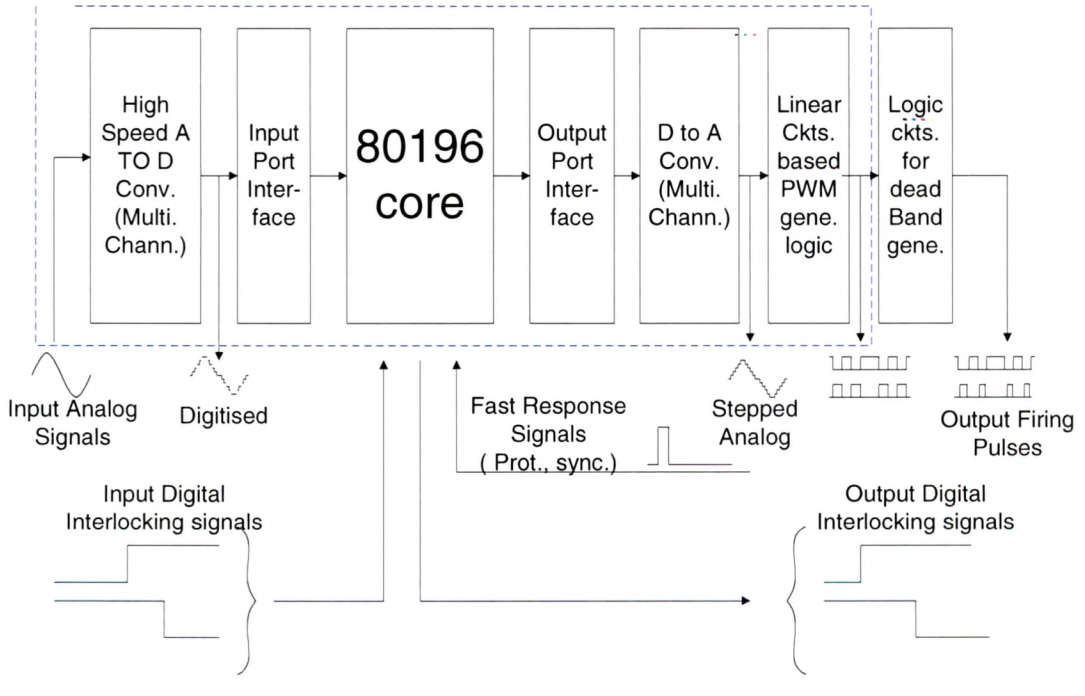


Fig. 4.3 Solution with MCS-96 based controller

4.2.4 SOLUTION WITH PC BASED CONTROLLER

While the solution can meet the requirements its usage for real time 24 x 7, 365 days needs, it is not economical from commercial product point of view.

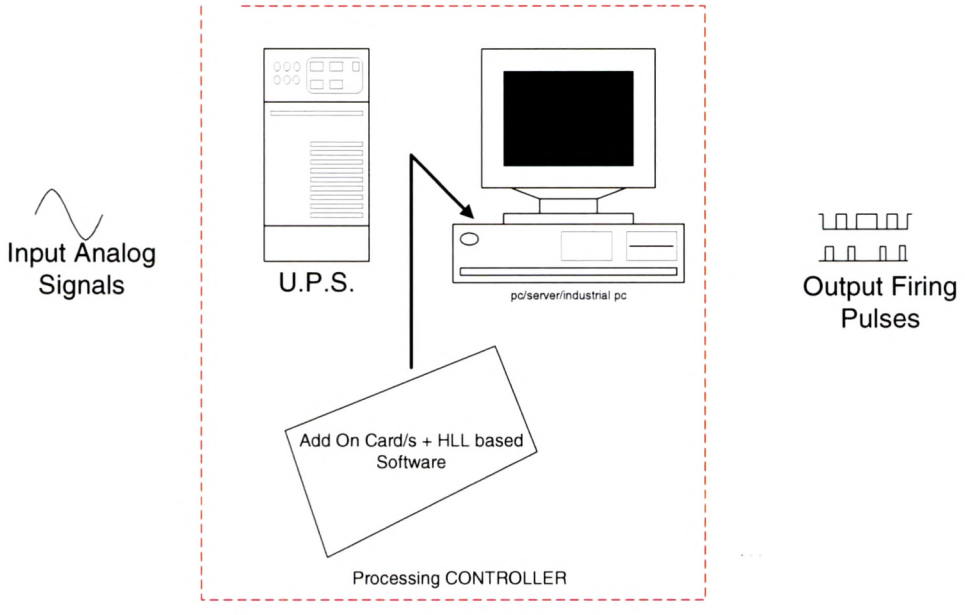


Fig. 4.4 Solution with PC based controller

4.2.5 SOLUTION WITH 24X BASED DSP

It can be seen (pink line) practically all the functional blocks including dead time generation circuit, can be integrated within single chip facilitating highly compact and robust integration.

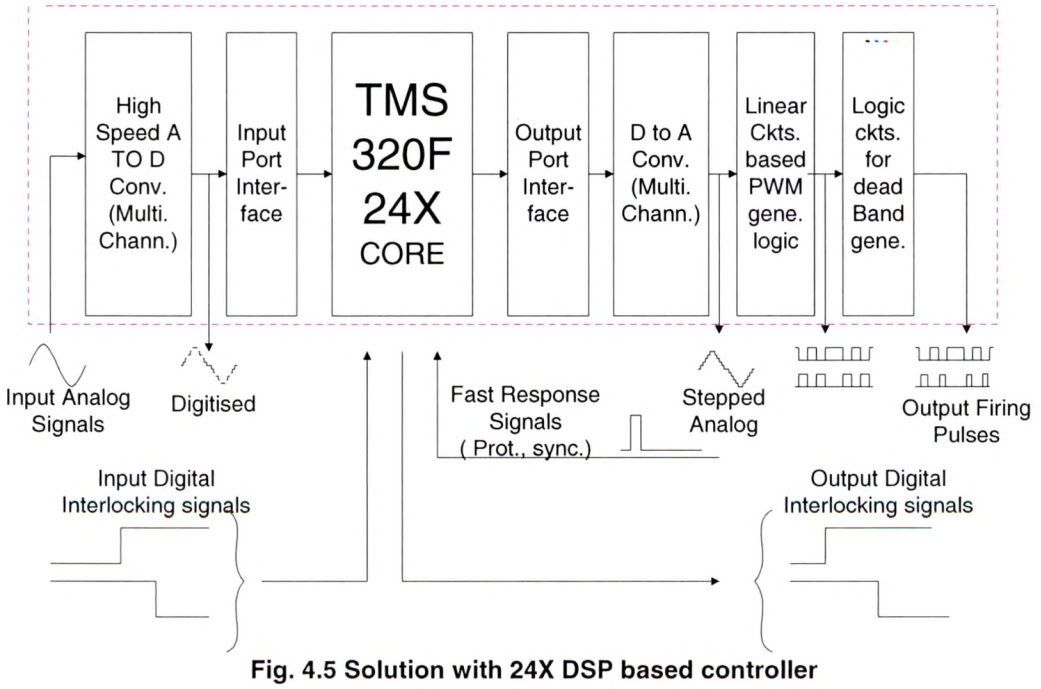


Fig. 4.5 Solution with 24X DSP based controller

4.2.6 SOLUTION WITH 24XX BASED DSP

This solution apart from the basic functionality can help in big way networked design in line with communicability or master slave control requirement apart from superior real time performance.

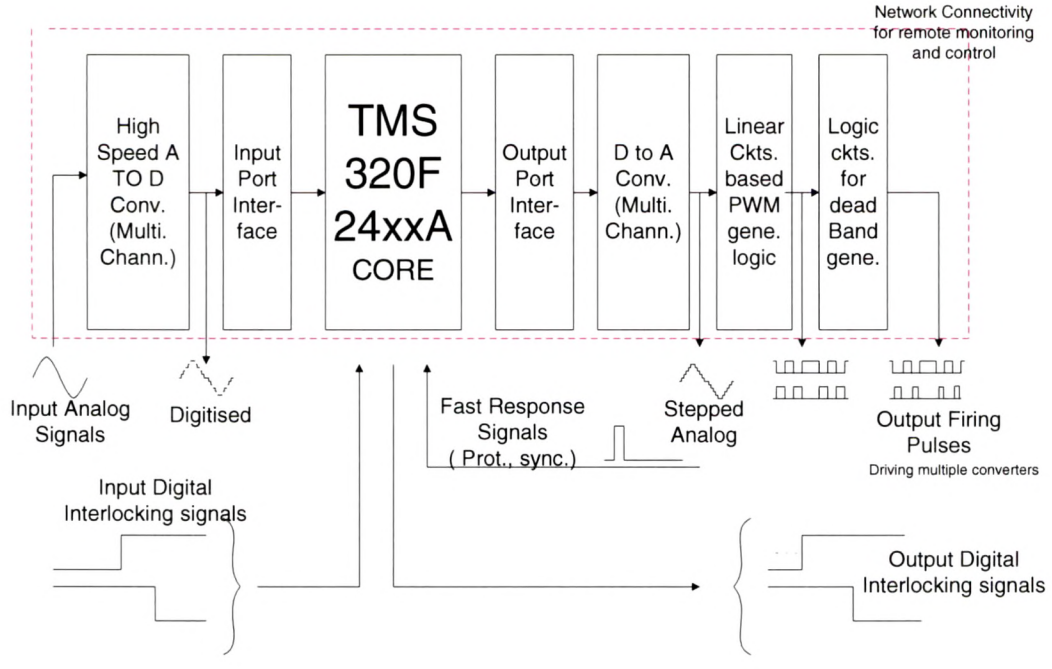


Fig. 4.6 Solution with 24XX DSP based controller

4.3 PHYSICAL DESIGN BASED ON MCS-96 CONTROLLER

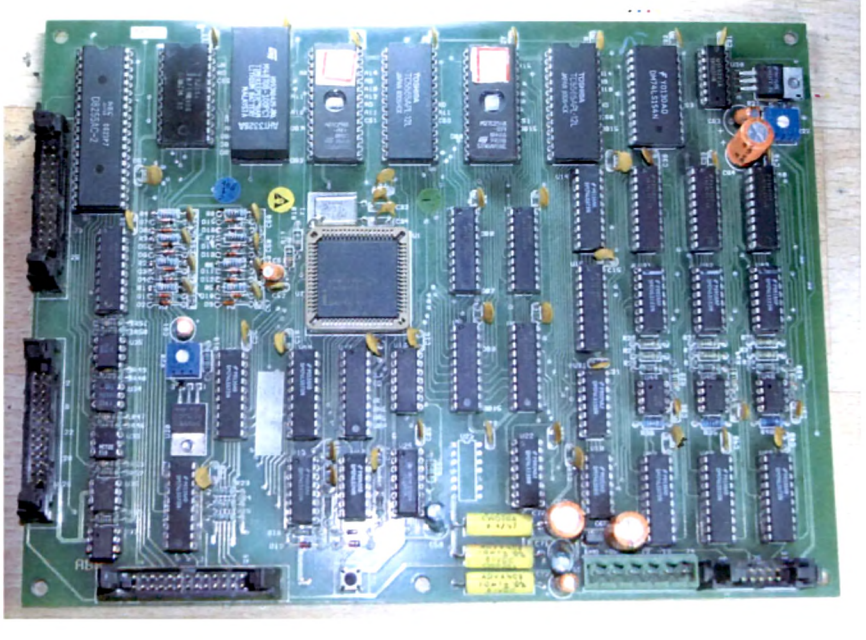


Fig. 4.7 Photograph of MCS-96 (80196) based controller

With this as backdrop, Initial design of STATCON is based on MCS196 family of microcontroller offering on chip A to D converter and high speed input and output facility. Photograph of the board developed is shown in fig 4.7.

The board designed has been heart of the entire STATCON. Failure in this card brings the STATCON operation to a grinding halt. To achieve the desired function, this card incorporates 16 bit Intel Micro-controller N80C196KC20 operating at 12 MHz. To achieve the desired core control function, micro-controller is assisted by its peripherals, which occupy the balance space on the board. Some of the key peripherals used include EPROM bank of 64K space, RAM of 16K space, NVRAM space of 8k, programmable peripheral interface, programmable timer, high speed Digital to Analog (D to A) converters, buffers for input signals and control regulators for reference feed to the analog section of the circuit.

The card receives the power supplies (+5V, +/-12V). It also receives analog and digital inputs and gives out analog and digital outputs. It receives the TTL logic buffered signals which include hold for the entire gate circuit firing pulse control (active low), main contactor "on" control (active high), start input enable (active high), bypass contactor "on" control (active high). The unipolar, conditioned analog signals (0-5V) are received from the analog card, which form the key control parameters for dynamic compensation. These include three-phase input voltages, three-phase load currents, dc bus voltage feedback and PI control value.

The digital status / control signals at TTL logic levels received by the card are buffered internally before being fed to core control circuit. This includes start contactor feedback contact, bypass contactor feedback contact, stop command from user through front panel pushbutton, zero crossing detector signal for dynamic frequency calculation, master fault input from the protection card, synchronizing signal corresponding to 'R' phase positive zero cross over, and negative zero cross over signals for all the three phases for facilitating their respective current measurements so as to derive corresponding phase reactive current component.

The final outputs (modulating signals) are in the form of dynamically computed 24 step waveforms for all the three phases with +/- 5V as peak amplitude in real time with appropriate phase relationship and in close synchronization with 'R' phase positive zero cross over. These signals are received by the analog card for further processing through sinusoidal PWM generation hardware to deliver the gate pulses to the IGBT's.

4.4 PHYSICAL CONTROLLER DESIGN UPGRADE WITH 24X DSP

Improved board with Texas 24x DSP (TMS 320LF240PQ) was designed with same boundary conditions and substituted with generation of 48 pulse waveform and achieving sub-cycle response. The block diagram of the DSP board and the photograph are shown in the fig. 4.8 and 4.9 respectively.

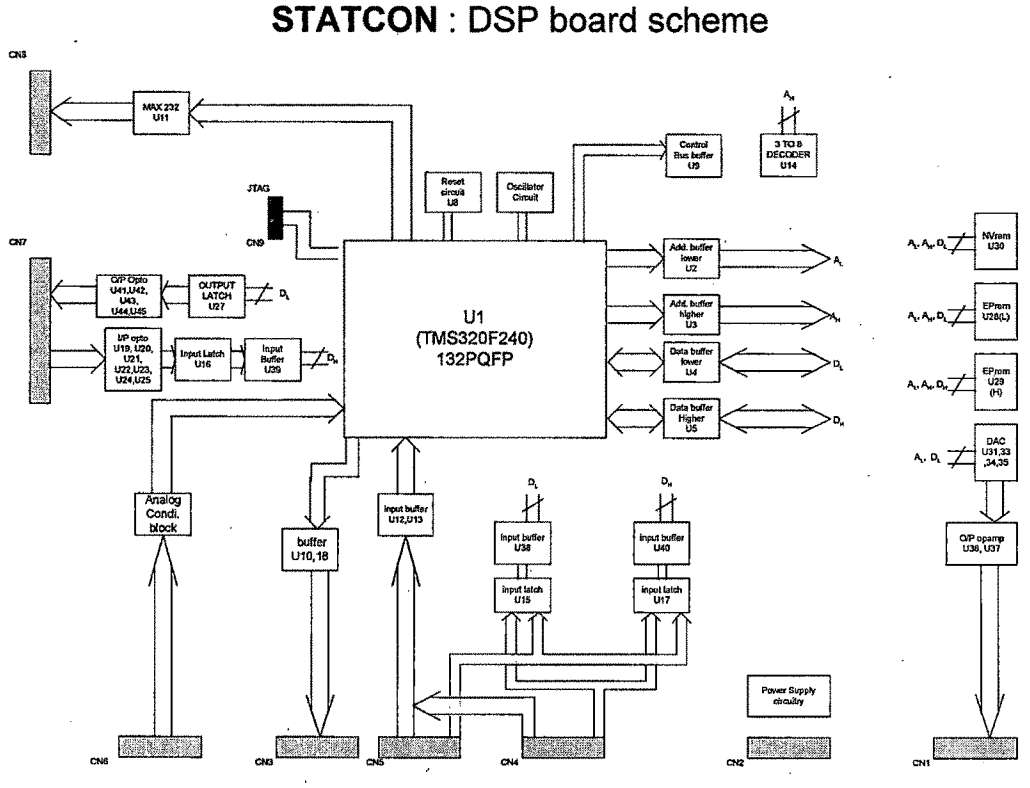


Fig. 4.8 Block diagram of TMS320LF240PQ based DSP controller

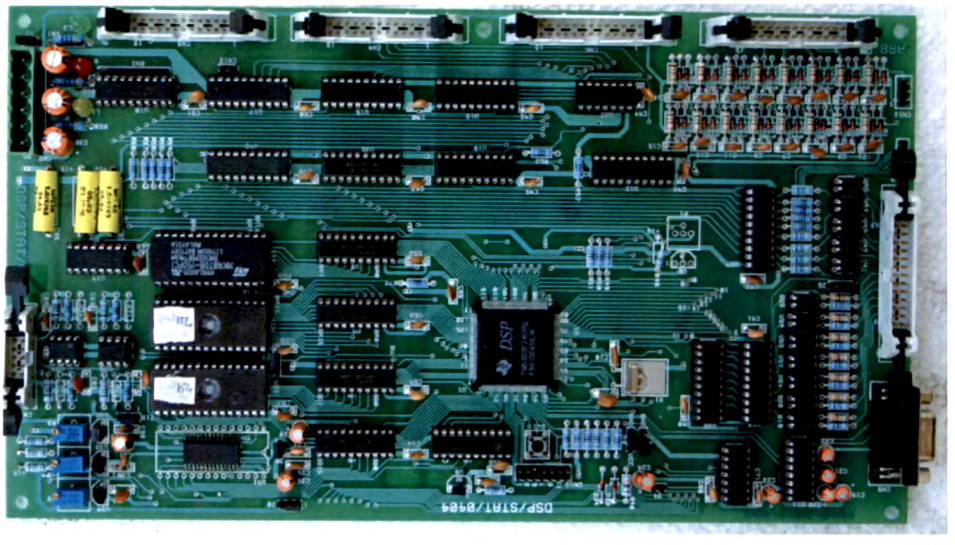
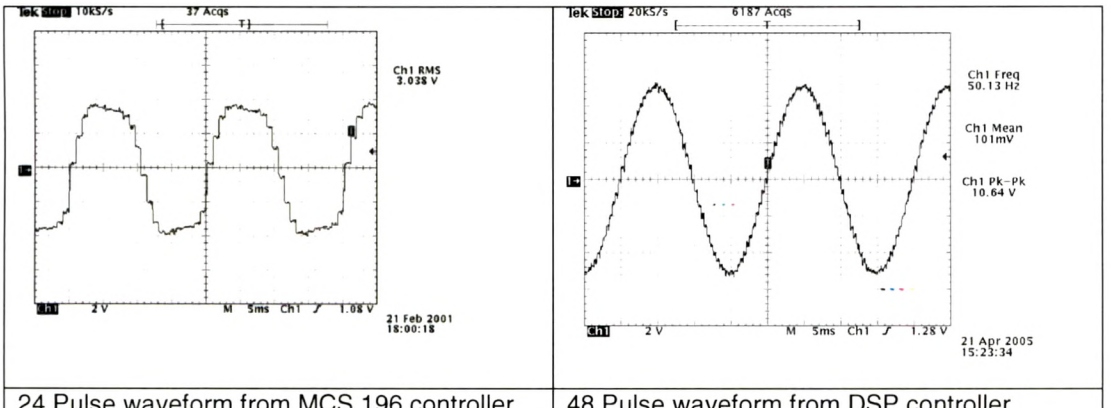


Fig. 4.9 Photograph of TMS320LF240PQ based DSP controller

The 24 pulse and 48 pulses output waveform for the MCS96 and Texas DSP board is as shown in below fig.



24 Pulse waveform from MCS 196 controller	48 Pulse waveform from DSP controller

Fig. 4.10 Pulse waveform from Digital controller

4.5 NEW GENERATION DIGITAL CORE DEVICES

In early 2000, various processors from different manufacturers for e.g. Texas Instruments- 24xx family of processors, Free scale 56800 and 56800E, Renesas SH7124 and SH7125 etc. having the peripheral modules, meeting current requirements of the digital controls started getting offered for commercial use in production. Their difference was in terms of the features offered apart from cost, speed, peripherals, power consumption etc. Latest available processors in this family with their features are compared in the table 4.1.

Prototype board based on TMS320LF2407A was also designed and few control requirements were taken up for further evaluation. The incremental advantage gained in this upgrade had been that the controller on chip flash can be programmed with simple serial utility facilitating on field programming and direct on chip PWM generation with analog to digital converter deploying digital sequencer and thereby optimal updating of analog parameters independent of the executing loop. Further with on chip generation of PWM, the offset related aspects associated with analog triangular carrier wave gets eliminated.

Photograph of 2407A prototype board is as below:

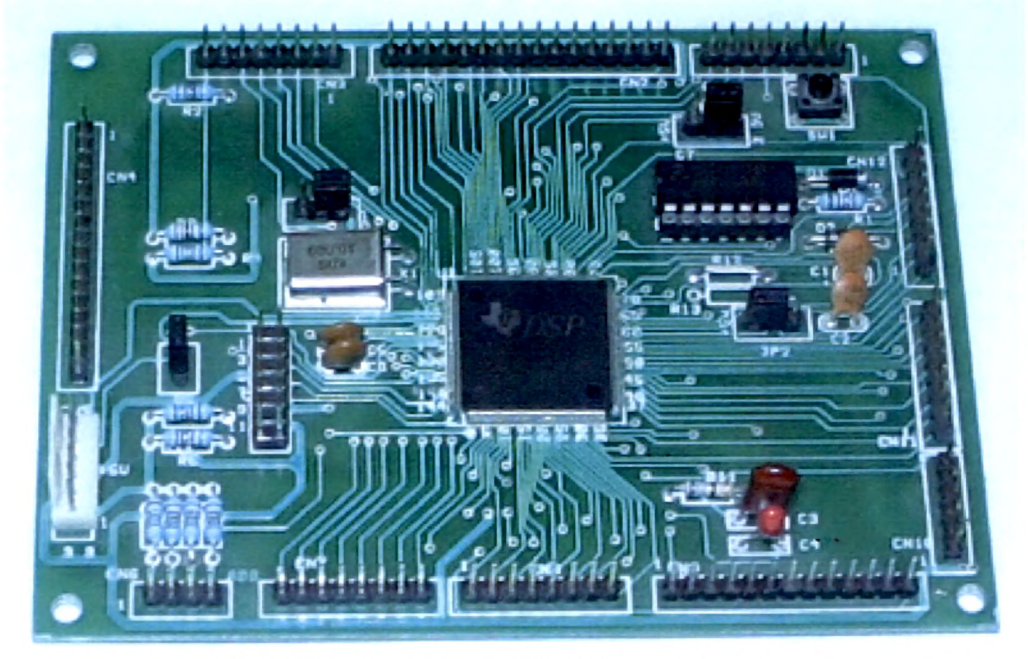


Fig 4.11 Photograph of 2407A DSP prototype board

Extended details of design are covered in [223]

Table 4.1 Features of 240x DSP family devices

FEATURE		LF2407A	LF2406A	LF2403A	LF2402A	LC2406A	LC2404A	LC2403A	LC2402A
C2xx DSP Core		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction Cycle		25 ns	25 ns	25 ns	25 ns	25 ns	25 ns	25 ns	25 ns
MIPS (40 MHz)		40 MIPS	40 MIPS	40 MIPS	40 MIPS	40 MIPS	40 MIPS	40 MIPS	40 MIPS
RAM (16-bit word)	Dual-Access RAM (DARAM)	544	544	544	544	544	544	544	544
	Single-Access RAM (SARAM)	2K	2K	512	512	2K	1K	512	—
3.3-V On-chip Flash (16-bit word) (4 sectors: 4K, 12K, 12K, 4K)		32K	32K	16K	8K	—	—	—	—
On-chip ROM (16-bit word)		—	—	—	—	32K	16K	16K	16K
Code Security for On-Chip Flash/ROM		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Boot ROM		Yes	Yes	Yes	Yes	—	—	—	—
External Memory Interface		Yes	—	—	—	—	—	—	—
Event Managers A and B (EVA and EVB)		EVA, EVB	EVA, EVB	EVA	EVA	EVA, EVB	EVA, EVB	EVA	EVA
--General-Purpose (GP) Timers		4	4	2	2	4	4	2	2
--Compare (CMP)/PWM		12/16	12/16	6/8	6/8	12/16	12/16	6/8	6/8
--Capture (CAP)/QEP		6/4	6/4	3/2	3/2	6/4	6/4	3/2	3/2
--Input qualifier circuitry on PDPINTx, CAPx, QEPx, XINT1/2, and ADCSOC pins		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
--Status of PDPINTx pin reflected in COMCONx register		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
10-Bit ADC		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
-- Channels		16	16	8	8	16	16	8	8
-- Conversion Time (minimum)		500 ns	500 ns	500 ns	500 ns	500 ns	500 ns	500 ns	500 ns

Table 4.1 contd...

FEATURE	LF2407A	LF2406A	LF2403A	LF2402A	LC2406A	LC2404A	LC2403A	LC2402A
SPI	Yes	Yes	Yes	—	Yes	Yes	Yes	—
SCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CAN	Yes	Yes	Yes	—	Yes	—	Yes	—
Digital I/O Pins (Shared)	41	41	21	21	41	41	21	21
External Interrupts	5	5	3	3	5	5	3	3
Supply Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Packaging	144-pin PGE	100-pin PZ	64-pin PAG	64-pin PG	100-pin PZ	100-pin PZ	64-pin PAG	64-pin PG, PAG
Product Status: Product Preview (PP) Advance Information (AI) Production Data (PD)	PD	PD	PD	PD	PD	PD	PD	PD

4.5.1 SOME OF THE IMPORTANT WAVEFORMS REALIZED THROUGH 2407A BOARD

4.5.1.1 120^{O} PHASE SHIFTED SINUSOIDAL PWM OUTPUT FOR THREE PHASE INVERTERS

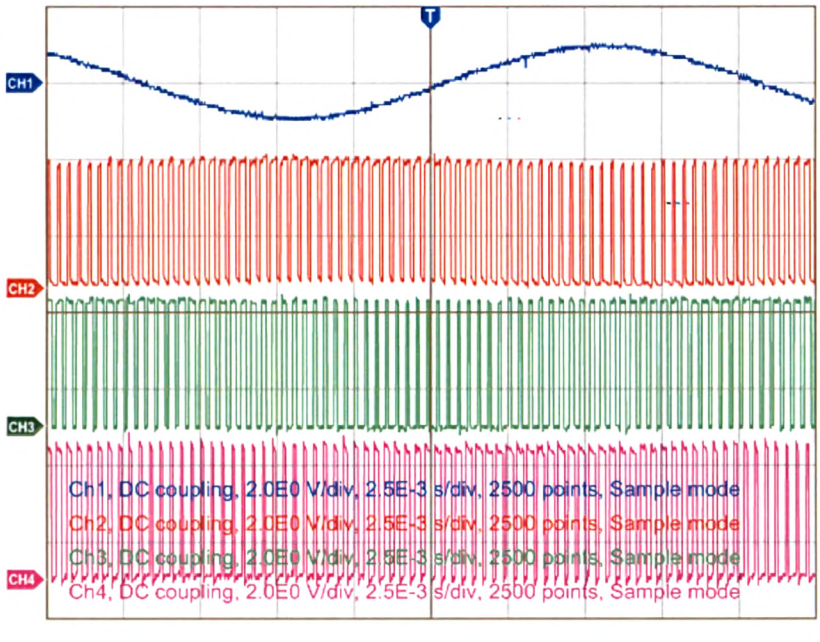


Fig. 4.12 120^{o} phase shifted sinusoidal PWM output for three phase Inverters

4.5.1.2 THREE PHASE PWM OUTPUT OF INVERTERS

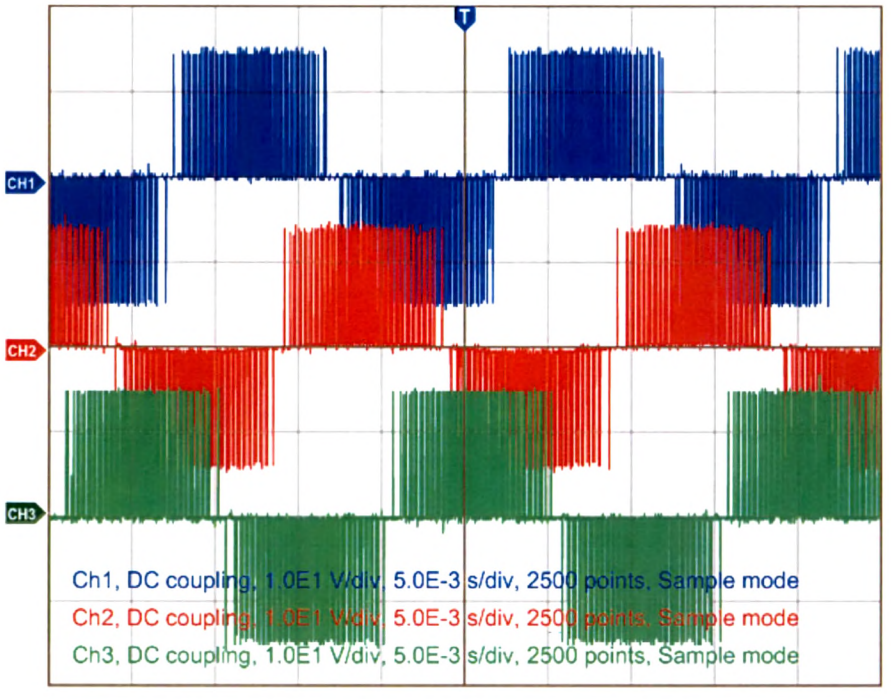


Fig. 4.13 Three Phase PWM Output of Inverters

4.5.1.3 PWM WAVEFORMS DEMONSTRATING DEAD BAND GENERATION

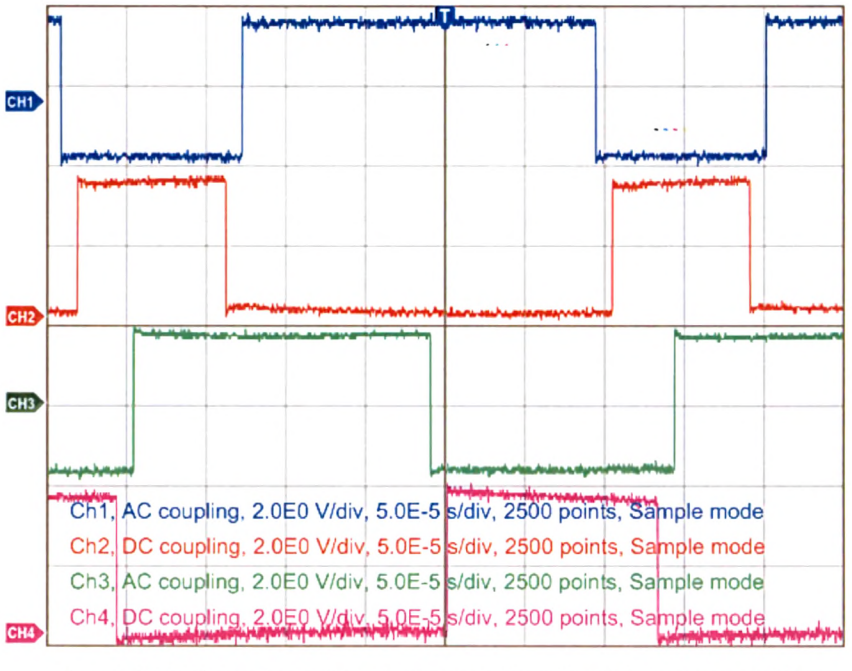


Fig. 4.14 PWM waveforms demonstrating dead band generation

In the waveform shown in fig. 4.14, CH1, CH2 shows the PWM and it's inverted with dead time for inverter bridge one and CH3, CH4 shows PWM generated for inverter Bridge two having carrier signal 90° phase shifted from carrier signal for bridge one.

4.6 LATEST OFFERINGS: TEXAS 28XX DSP

Further in terms of latest offerings is Texas 28xx family of devices. With this family of devices feature like carrier cancellation for parallel converter operation can now directly be achieved offering very large scale hardware reduction and directly facilitating reduction of associated wiring lengths and better EMC compatibility. Current spectrum of the processors available for such kind of application is also listed in the table 4.2. Some of enhancements in 28XX family of DSPs for power electronic applications are listed in following section.

4.6.1 DETAILS OF TMS320F2812 PWM GENERATOR

Event manager unit incorporating, pulse-pattern-generator circuit, for programmable generation of asymmetric, symmetric, and four-space vector PWM waveforms with programmable dead band generator and up to 8 PWM waveform can be generated simultaneously by each event manager (two event manager are available). It also supports double update PWM mode with reloading on underflow (beginning of PWM period) OR period (middle of PWM period). Also PWM pin toggling frequency is limited by the GPIO output buffer switching frequency (20 MHz) min pulse duration (on/off) = 25 nSecs.

Similarly, enhancement of Analog to Digital (A to D) converter is there and it is now 12-bit A to D core with built-in-Sample and Hold (S/H) and fast conversion rate: 80ns at 25 MHz with A to D clock(12.5 MSPS). Further, it can be operated in simultaneous sampling mode and sequencer sampling mode. This also supports, auto sequencing, "start/stop" mode, sequential override, dual and cascaded mode along-with analog input of 0.0 V to 3.0 V with voltages above 3.0 V producing full-scale conversion results.

Table 4.2 : Devices with features optimized for Power Electronics applications										
	TEXAS INSTRUMENT	ANALOG DEVICE			FREESCALE SEMICONDUCTOR	MICROCHIP	PHILIPS	RABBIT SEMICONDUCTOR	RENESAS SEMICONDUCTOR	ATMEL
Sr. No.	TMS 320 F 2812	Blackfins ADSP BF-549	Sharc ADSP-21369 BSWZ-1A	ADSP 21990	MMC2114 M•CORE	PIC 32	LPC2138	rabbit 4000	M308B8FGGP	AT91SAM 32-bit ARM-based Microcontrollers
Generation	tms320f28xx	ADSP BF-5xx	ADSP 21369 xxxx	ADSP 21xx	MMC2114 M•CORE	PIC32 MX460F512L	LPC21xx	rabbit xxxx	M32C/8B	AT91SAM7A3
PE APPL.	CONVINIENT			CONVINIENT		CONVINIENT	CONVINIENT		CONVINIENT	CONVINIENT
PWM	16-Ch	11	16-Ch	6 + 2(AUX.)		5	6	4	5	8
ADC	16-Ch	NA		8-Ch	10-bit 8-channel	16 Ch	16 - Ch	NA	10 bit , 34 channel (in single chip mode)	16 Ch
Interrupt	45 (peripheral), 3 (external)			17 (3-internal,2-external,12-user define	up to 43	5 (external interrupt)	9 (external interrupt)	4	11 (on single chip mode)	11 (on chip mode)
GPIO	56	Up to 152	16 muxed flag	16 bidirectional multifunctional flag	up to 104	85	46	40 and more	121	62
CAP/QEP	6/2	/2		AVAILABLE	4	5	4	2/2	3	AVAILABLE
Frequency (MHz)	150	533	400	160	50	80	30	60		60
Timers	3 x 32-bit GP	11 x 32-bit GP,	3 GP	3 x 32 bit GP	2	5 x 16 bit, 1 x 32 bit	2 x 32-bit	10 x 8-bit;1 x 10-bit up down counter,1 x 16-bit	11 x 16 bit	9 x 16 bit
UART	1	4	2	Y	2	2	2		5	3 enhanced USART
SPI	1	Up to 3	2	Y	YES	1	2	4		2
CAN	1	Up to 2	N	N		N	2			2
FLASH	256 KB	N		N	256 Kbytes	512 KB	256 KB		2x 4 KB (in flash memory version only)	256 KB

4.7 SALIENT FEATURES OF EMBEDDED SOFTWARE OF DIGITAL CONTROLLER FOR SINGLE AND THREE-PHASE STATCON PANELS

Entire STATCON real time control operation is achieved through software written completely in assembly language (residing in the EPROMs/ on chip flash of the Digital card), to help execute the following

1. 166 nsecs. is the processor operating time base with majority of the instructions getting executed @ 4 such states for 80196 controller based hardware.
2. Frequency computation is done to the second order of decimal. It is updated at every cycle. System latches on the frequency value at the start up as reference and accepts 0.2Hz (programmable) deviation per cycle. This ensures healthy operation and dynamic frequency updates even in noisy environment once the power stack is charged and IGBT's are fired.
3. Respective phase voltages are computed with appropriate correction factor from the available analog signal corresponding to the peak of incoming voltage and are also computed to second order of decimal for accurate processing. These voltage updates are achieved once in a cycle for each phase. Based on start up voltage condition, dynamic limits for the phase voltage magnitudes are computed so as to prevent the system from accepting unwanted voltage magnitudes outside the limits in presence of noisy environment once the power stack is charged and the IGBT's are fired.
4. The reactive component of current corresponding to each phase is also calculated based on the magnitude of the conditioned analog current signals available from the analog card for each phase. For balanced loads single current feedback is adequate. However, the provision is there to accept all the three-phase current feedbacks. The compensation by STATCON then can be based upon minimum OR maximum OR average of the reactive current components of the three load currents. These current updates are also done once in each cycle. However, rate of change of current effective to be offered by STATCON for compensation is programmable. This is an essential feature of the STATCON which is decided by an application demanded response and also to avoid excess current jerks on IGBT's as well as Electro Magnetic Interference (EMI) jerks in the given environment. Based on rate of change current value permissible, the limits for current

are computed once the STATCON current value is given out starting from "zero as initial value". If the phase relationship, i.e. In case of inductive to capacitive or vice versa, gives cross over, the system forces current change through zero at the permissible rate of change.

5. The dynamic PI value is also accepted by the controller and is mapped with appropriate magnitude while solving the control equations based on current, voltage, frequency values for each phase. The PI value is also accepted within set limits and is updated minimum three times during each cycle.

6. The dc bus voltage also is updated once in the cycle and is used as a factor [2 – (dc voltage actual / dc voltage reference)] during capacitor voltage buildup and then as important protection parameter during the dynamic operation of STATCON.

7. To ensure proper synchronization, 'R' phase positive zero cross over is used as the sync signal trigger and this trigger is accepted only in the last step of the 24/48 step calculation (i.e. between 345 to 360 degrees) and when the 24/48th step waveform has already been given out. Also to overcome EMI effect, if any, on receipt of the trigger signal, the physical condition of zero cross over is also verified by the micro-controller before accepting it as the valid signals.

8. System divides the entire control cycle in the form of 24/48 steps and at each step it updates the modulating signal values for each phase with the last updated parameters (voltage, current, PI, frequency).

9. Depending upon the modulating signal step number, one update or calculation related job is also executed by the micro-controller. This job can be any one of the following.

- Voltage updates for R phase
- Voltage updates for Y phase
- Voltage updates for B phase
- Current updates for R phase
- Current updates for Y phase
- Current updates for B phase
- DC Bus voltage update
- PI value update (multiple updates)

- Frequency value update
- STATCON compensating current value update based on the maximum / minimum / average etc. as required by the load application logic
- Current dynamic limits calculation

10. The left over time during each step is utilized for protection checks, such as, abnormal dc bus voltage, start contactor withdrawn, stop signal activated, and presence of fault signal.

In single phase application, except the computation for phase Y and B are substituted by additional updating efforts for dc bus and PI values on the input side and the output modulating signals for these phases carries replica of R phase only and thereby facilitating independent direct feed to the paralleled IGBT Stack, drive circuits.

Followed in next sections are the case studies of STATCON installations in automobile industry and railway application in India.

4.8 STATCON INSTALLATION FOR SPOT WELDING APPLICATIONS

This section includes practical experiences on the execution of a 3*600 kVAR IGBT based dynamic reactive power compensation system employed for spot welding application in a car plant. Spot welding being a highly dynamic, unpredictable, and unbalanced load requires equally fast acting reactive power compensation. The experiences lead to recommendations for hardening the functional designs for EMI mitigation with special techniques, while achieving the targeted responses of the system in actual field operation.

4.8.1 DETAILS OF SPOT WELDING SYSTEM SOLUTION

The car plant spot welding facility in automobile industry in India consists of a shop floor (20000 sq.mt.). This houses number of spot welding guns with capacities ranging from 40 kVA to 120 kVA and working on two-phase supply. The entire welding load is fed from three identical capacity transformers located in nearby substations. The nominal supply frequency is 50 Hz. Each transformer is 22 kV / 415 V with 2 MVA rating. It is Δ / Y connected with secondary side neutral grounded near the transformer itself. The available short circuit capacity on the secondary side of the transformer is 35 MVA. The existing transformers have already been loaded almost to

their full capacities. The expansion of the spot welding facility hence demanded approximately 600 kVAR compensation per transformer. This demand could have been met with a new substation of 22KV/415V, 2MVA transformer. However, it meant heavy expenses and space. Installation of a dynamic reactive power compensation of 600 kVAR per transformer, hence was targeted as solution approach.

4.8.2 600 KVAR DYNAMIC COMPENSATION SYSTEM PER TRANSFORMER

The spot welding load is a highly unpredictable and also highly unbalanced load. Thus, each phase needs separate reactive power compensation. The per phase 0 to 200 kVAR variable compensation deployed, hence uses:

- 100 kVAR fixed capacitor bank
- 100 kVAR IGBT based full bridge Voltage Source Converter (realized through STATCON)

STATCON i.e. 100 kVAR IGBT converter can work in inductive and capacitive mode (non simultaneous operation). It can, hence, offer 0 to 200 kVAR dynamic compensation at all the times. It is further split into two numbers of 50 kVAR converters operating in parallel since the basic design is of 50 kVAR, as a complete working product; including the switchgear, power converter, control logic and control electronics.

The single line diagram of the transformer supplying the spot welding loads and the compensation system employed is given in fig. 4.15. This is identical for all the three transformers. The total compensation for three transformers put together is 1800 kVAR. The important point to be noted here is that the load side current feedback could not be obtained / implemented directly due to substation load distribution panel layout. The source side current feedback, hence, was considered.

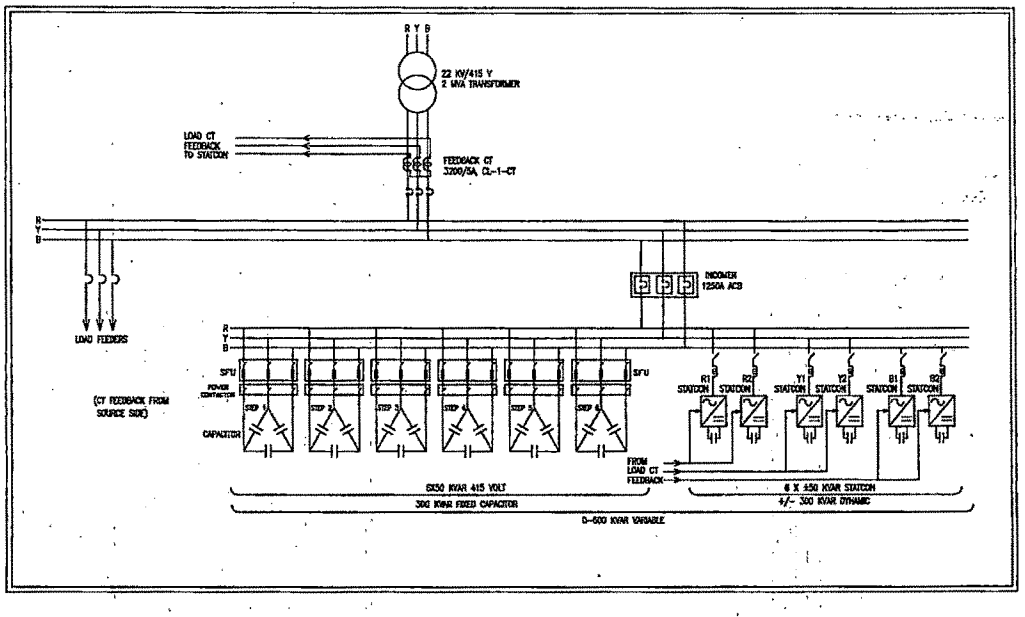


Fig 4.15 The single line diagram of the transformer supplying the spot welding loads and the compensation system employed

The power scheme for each of the 50 kVAR converter is given below in fig. 4.16.

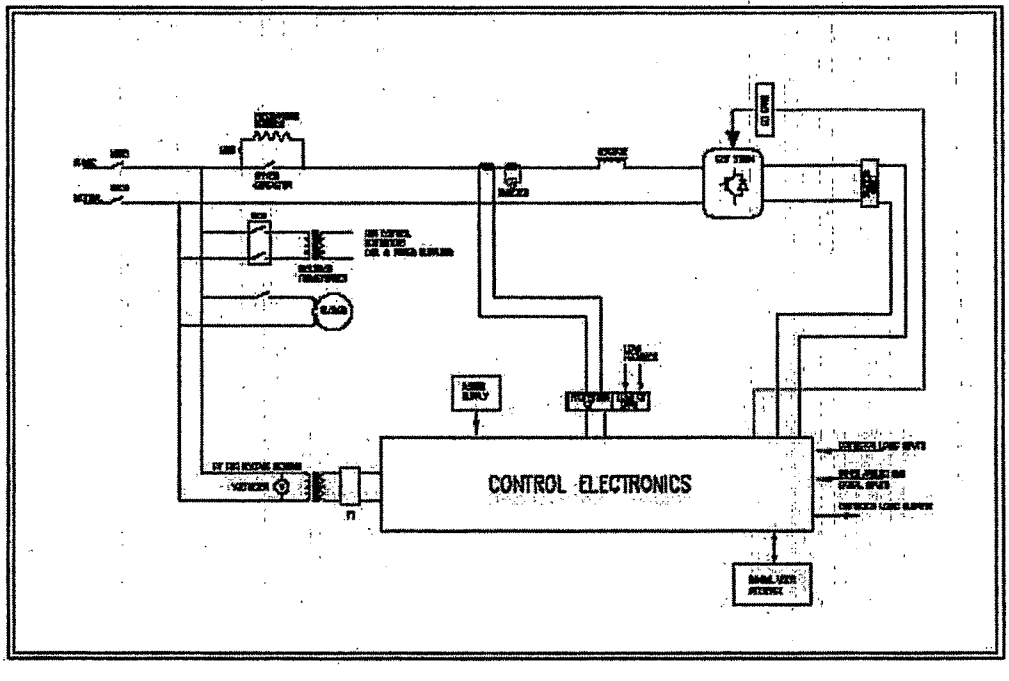


Fig. 4.16 Power scheme for each of the 50 kVAR converter

4.8.3 CONTROL IMPLEMENTATION

The Control Electronics schema deployed is shown in fig. 4.17. A separate grounding is considered as a must for the compensation system connected to each of the transformer.

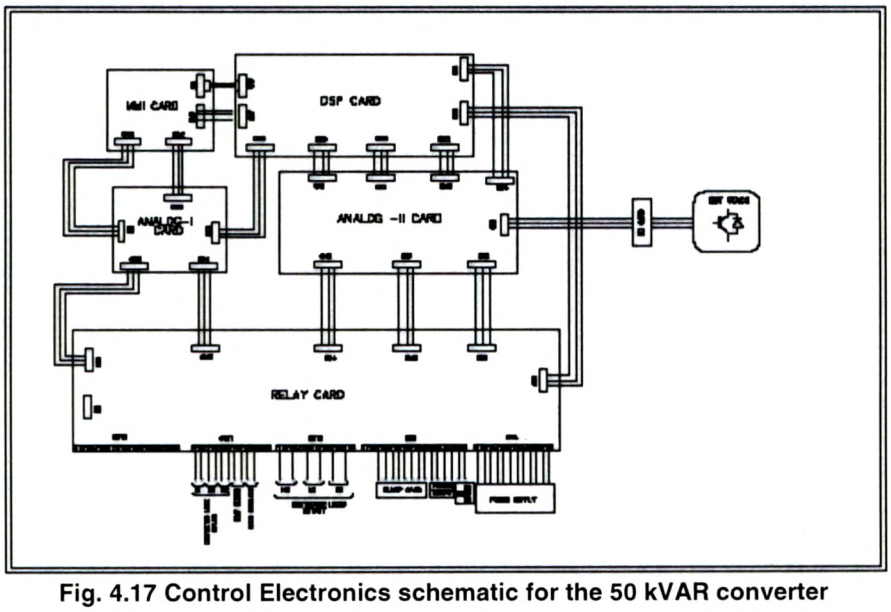
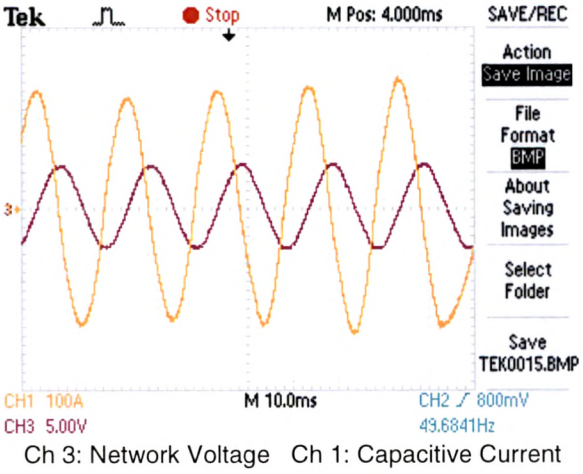


Fig. 4.17 Control Electronics schematic for the 50 kVAR converter

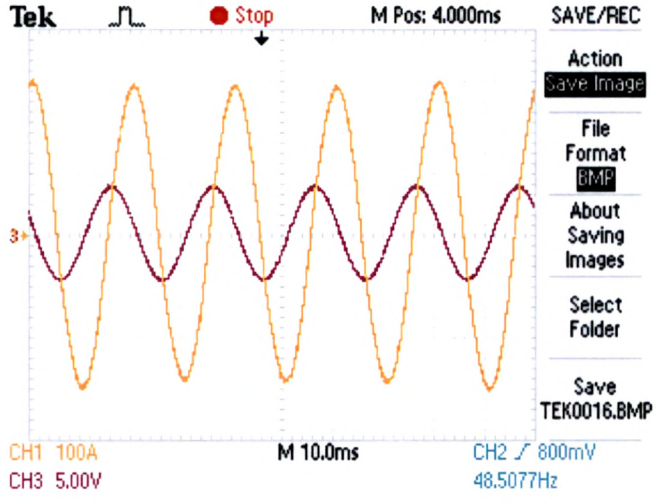
4.8.4 COMPENSATION WAVEFORMS

With the help of referred installation, STATCON compensation waveform for capacitive current is shown in fig. 4.18 and inductive compensation is shown in fig. 4.19



Ch 3: Network Voltage Ch 1: Capacitive Current

Fig. 4.18 Compensation for capacitive current

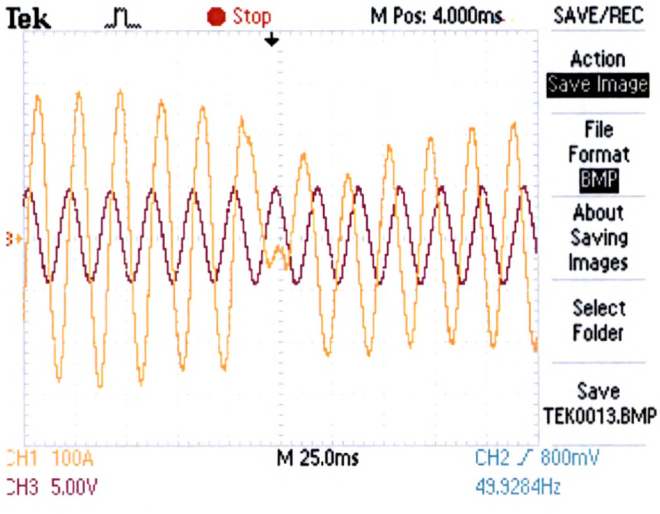


Ch 3: Network Voltage Ch 1: Inductive Current

Fig. 4.19 Compensation for inductive current

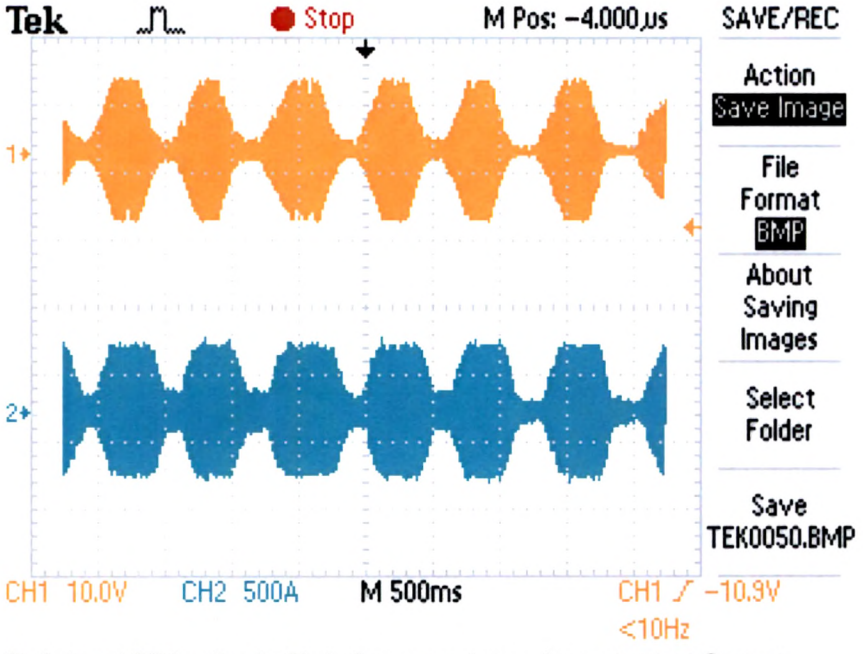
4.8.5 DYNAMIC RESPONSE OF STATCON COMPENSATOR

The important character of IGBT base Voltage Source Converter (VSC) based Dynamic Reactive Power Compensation is the "Dynamic response" so that, the incoming transformer does not get loaded with reactive power component at any moment and additional kVA is made available in the same transformer by maintaining unity PF operation. Fig. 4.20 and fig. 4.21 shows the dynamic response, which is close to one power cycle.



Ch 3: Network Voltage, Ch 1: Compensator current changes from capacitive to inductive within one cycle

Fig. 4.20 Dynamic mode change over response



Ch 3: Load CT feedback, Ch 1: Compensator equipment output Current

Figure 4.21 Dynamic multi cycle burst response

4.8.6 SUMMARY OF PERFORMANCE

Incase of two-phase supply based welding guns / single-phase loads, three phase transformer gets loaded with highly unbalanced currents and hence single phase IGBT based real-time/dynamic reactive power compensation system acts as important solution for dynamic power factor correction. The complete system with 18 numbers of 50 kVAR compensators (2 MVA, three transformers with 6 numbers of 50 kVAR single-phase compensators) and 900 kVAR capacitor banks hence was commissioned. The system thus offers 0 to 1800 kVAR dynamically variable reactive power to compensate the load reactive power demand. After commissioning this 1800 kVAR system, the transformer currents came down from Peak 2800 A (2000 A avg.) to Peak 2000 A (1400A avg.) approximately. This allowed for increased numbers of spot welding guns once again, apart from saving cost for three substations. The objective of saving cost of additional substation with increased spot welding capacity with the same transformers has thus been

realized. Extended details are covered in [224]. Vital design related aspects encountered during installation are listed later in chapter.

4.9 INSTALLATION FOR RAILWAY SUBSTATION APPLICATION

Railway traction in India deploy single-phase 66 /25 kV or 110/25 kV or 132/25 kV or 220/25 kV in Traction Sub-Station (TSS) for supplying power at 25 kV for electric traction loads. Traction loads have a high load dynamics. Traction loads usually inject lower order harmonics into the network. Further, conventional fixed shunt capacitor banks alone cannot maintain a good power factor at the incoming supply lines due to load dynamics.

To achieve good power factor nearing unity to avoid penalty (for lagging or leading poor power factor), to gain the better power factor benefits in the electricity bills, to reduce the maximum demand and applicable charges in the electricity bills, and to improve power quality, the sub-stations need to employ dynamic reactive power compensation equipment. The equipment needs to be connected on the 25 kV network and dynamic compensation of traction load reactive power is to be achieved using either Thyristor Controlled Reactor (TCR) or Thyristor Switched Capacitor (TSC) or IGBT based real-time advanced dynamic reactive power compensator.

The experiences on installation of the first IGBT based advanced real-time, smooth, and dynamic reactive power compensation system in Tractions Sub-Station (TSS) is now covered below.

Considering the traction load dynamics and presence of lower order current harmonics, an hybrid solution is employed to compensate both. This sub-station particularly demands 600 kVAR as the base capacitive type reactive power and 600 to 3000 kVAR as the dynamically varying capacitive type of reactive power for the traction load inductive power compensation. Thus, a total of 1800 kVAR Fixed Capacitor based compensation is first provided at 25 kV directly. The capacitor banks are basically de-tuned filter capacitor banks and offer maximum harmonic filtering effect at 25 kV itself.

Secondly, an IGBT based real-time, smooth, and dynamic reactive power compensator connected at 25KV through a step-up transformer is used to provide +/- 1200 kVAR compensation. It provides either capacitive or inductive type of reactive power. Thus in

association with fixed Capacitor banks of 1800 kVAR on 25 kV side, the total compensation provided is variable between 600 to 3000 kVAR (capacitive type) as required by the sub-station.

4.9.1 SCENARIO BEFORE INSTALLATION

Till 2004, railways used Fixed Shunt Capacitor Banks (FSCB) at Traction Sub-Stations (TSS) for improving power factor. The fixed shunt compensation always leads to either over or under compensation since the traction load is a dynamic in nature.

Before commissioning of the STATCON based Dynamic Reactive Power Compensator (DRPC) system, load (kVA) variation is shown in fig. 4.22, kVAR variation is shown in fig. 4.23, power factor variation is shown in fig. 4.24, and Total Harmonic Distortion (THD) is shown in fig. 4.25 for the TSS.

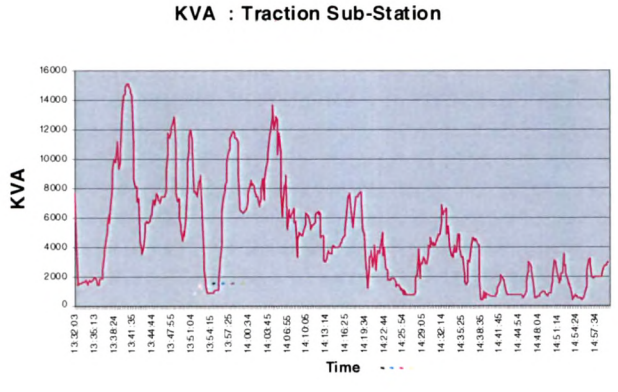


Fig. 4.22 kVA variation before compensation

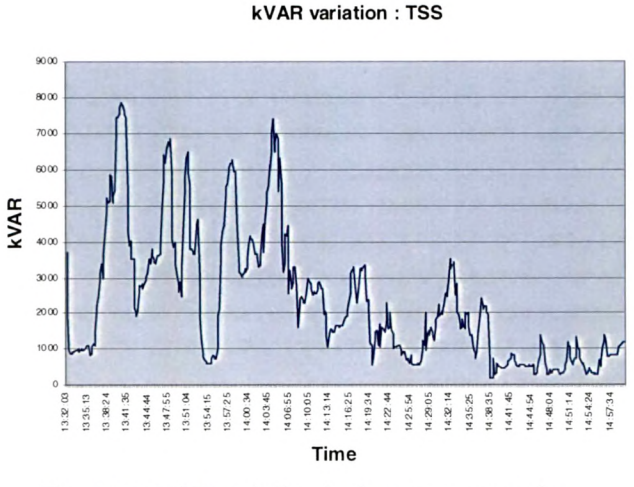


Fig. 4.23 kVAR variation before compensation

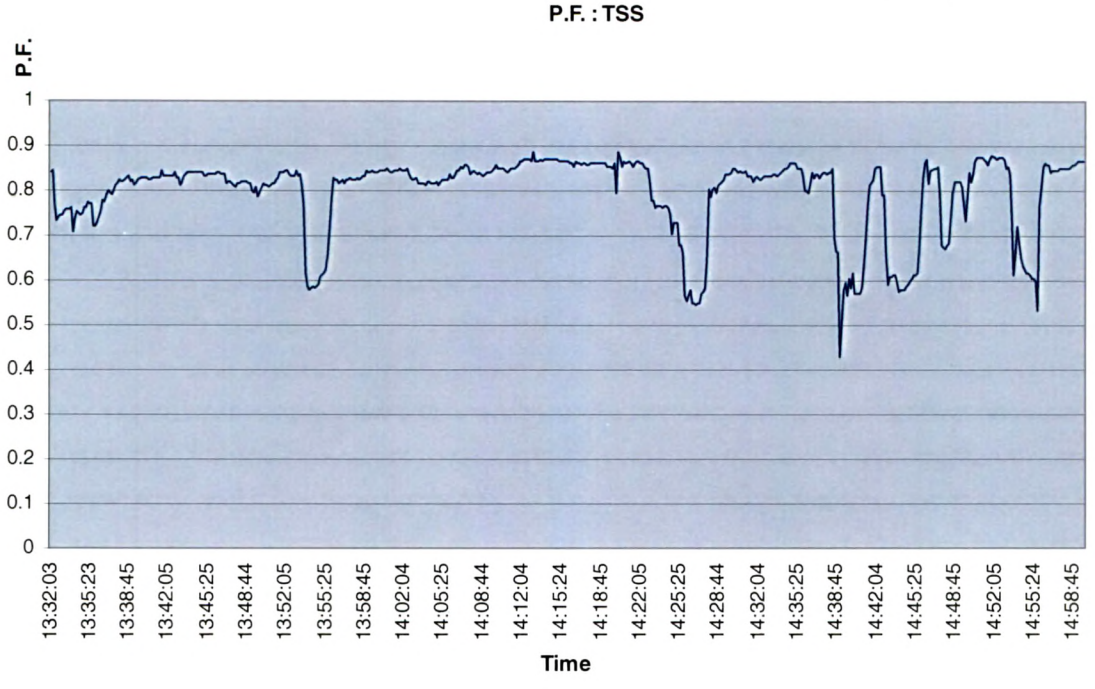


Fig. 4.24 Power factor variation before compensation

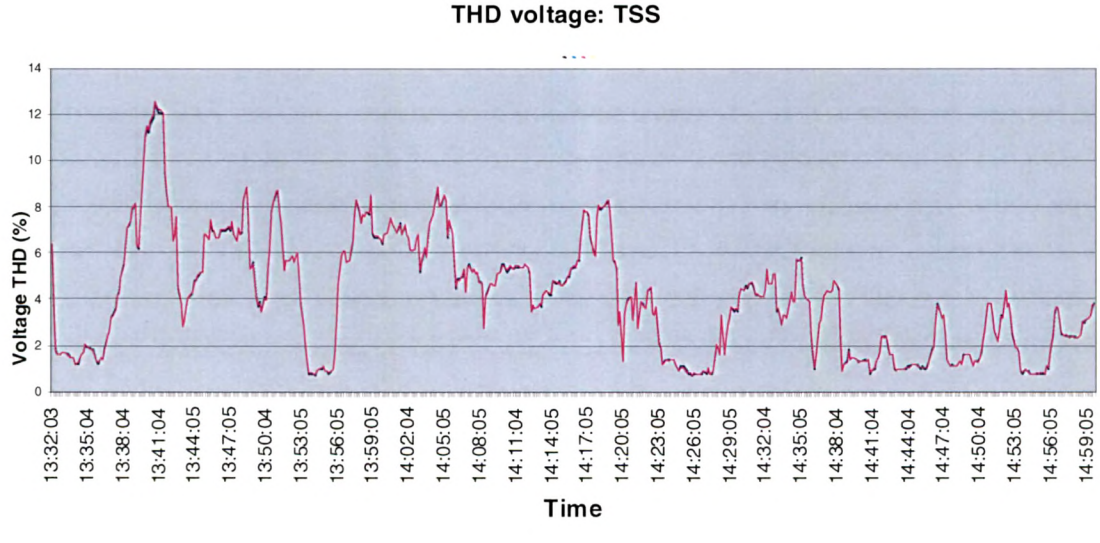


Fig. 4.25 THD variation before compensation

4.9.2 DRPC INSTALLATION

System installed covers the following.

- 1800 kVAR Fixed Capacitor compensation on HT side, with 13% series reactor for harmonic reduction.
- 25 kV/430V, 1600 kVA, Single phase transformer for connecting the IGBT based VSCs on low voltage side
- ± 1200 kVAR IGBT based singe-phase VSCs

Total compensation realized is 600 to 3000 kVAR

The single-phase STATCON supplied had been with rating for individual panel 430V, ±150 KVAR.

Thus, eight numbers of VSC or STATCON units are employed to achieve the required ± 1200 kVAR as mentioned above as shown in fig 4.26. If the load reactive power requirement varies from 600 to 3000 kVAR, this system will maintain zero reactive power demand from the grid. Also fig. 4.27 gives 3D view of the DRPC installation and fig. 4.28 gives 3D view for STATCON installation.

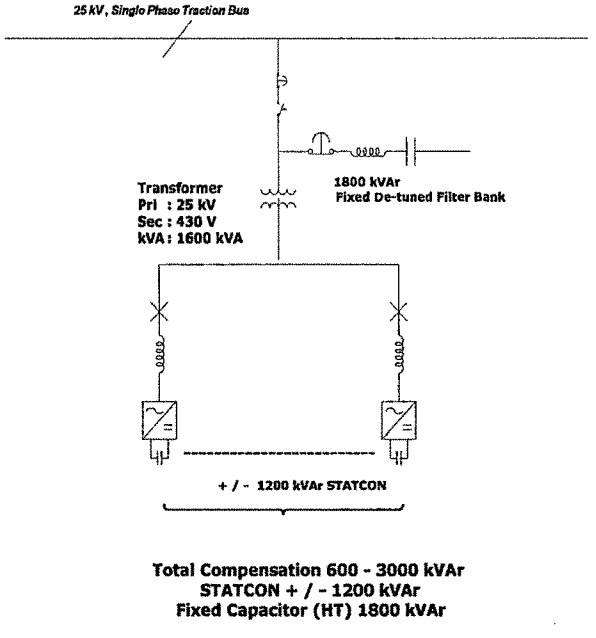


Fig. 4.26 600-3000 kVAR DRPC

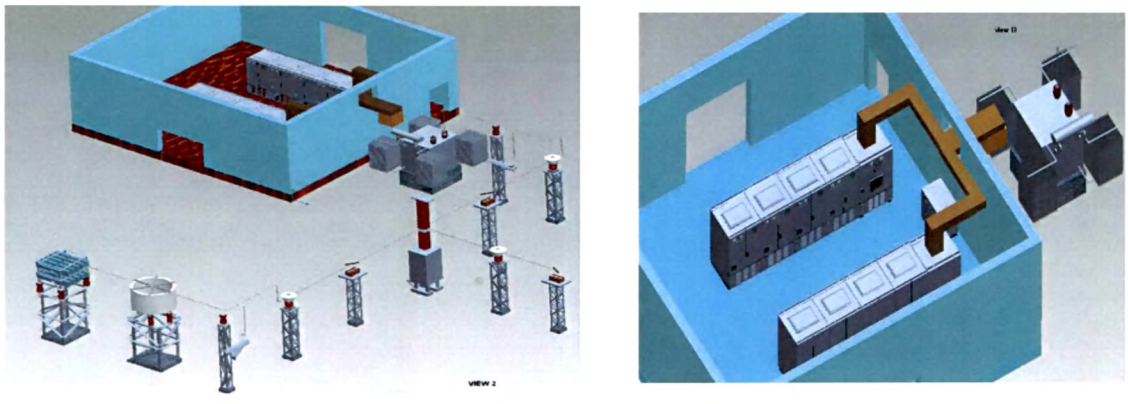


Fig. 4.27 3D view of Railway DRPC installation

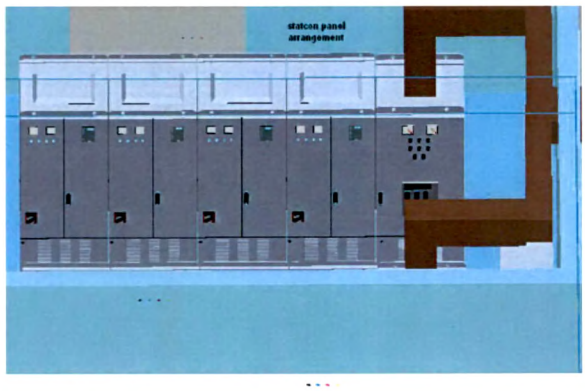


Fig. 4.28 3D view of STATCON installation

4.9.3 PERFORMANCE IMPROVEMENT IN RAILWAY TSS

Commissioning of the system helps maintain the power factor close to 0.93-0.94 every month (against the requirement calling for power factor of minimum 0.9) for the installation. Shown in fig. 4.29 is kW, kVA and kVAR variation, in fig. 4.30 is power factor variation, in fig. 4.31 is voltage THD variation, and in fig. 4.32 is Bus Voltage variation with and without the DRPC based compensation. Fig. 4.31 also which shows that load power factor is maintained close to 0.98 at 25 kV after the DRPC system is installed.

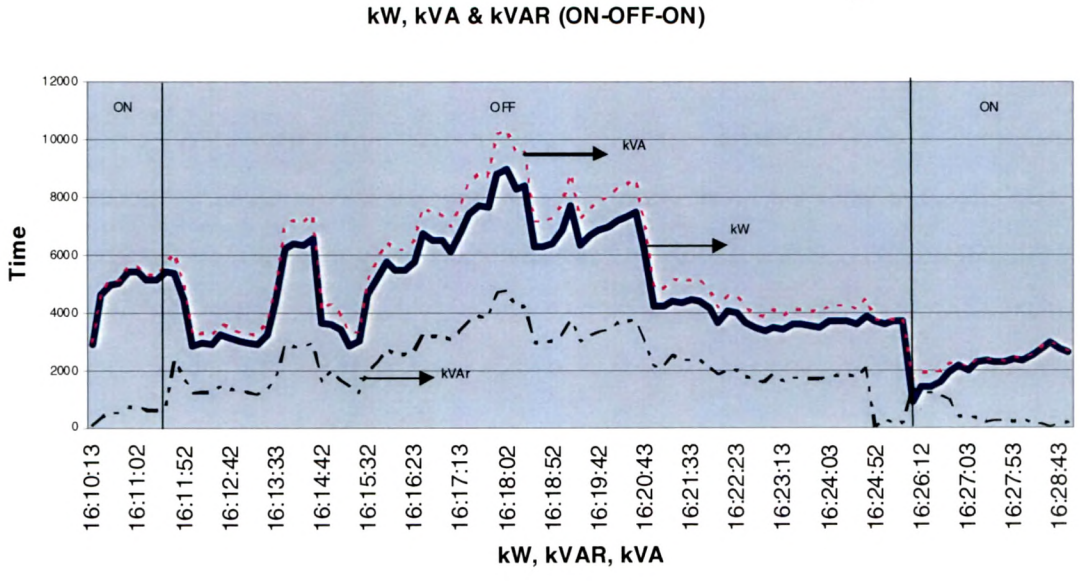


Fig. 4.29 kW, kVA and kVAR variation with and without compensation

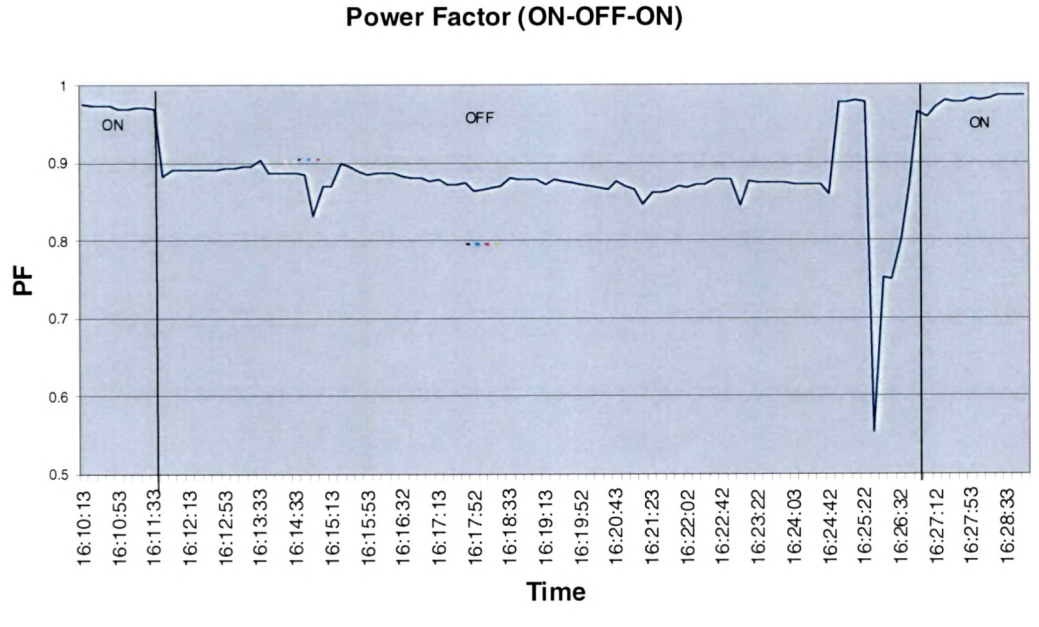


Fig. 4.30 Power factor variation with and without DRPC compensation

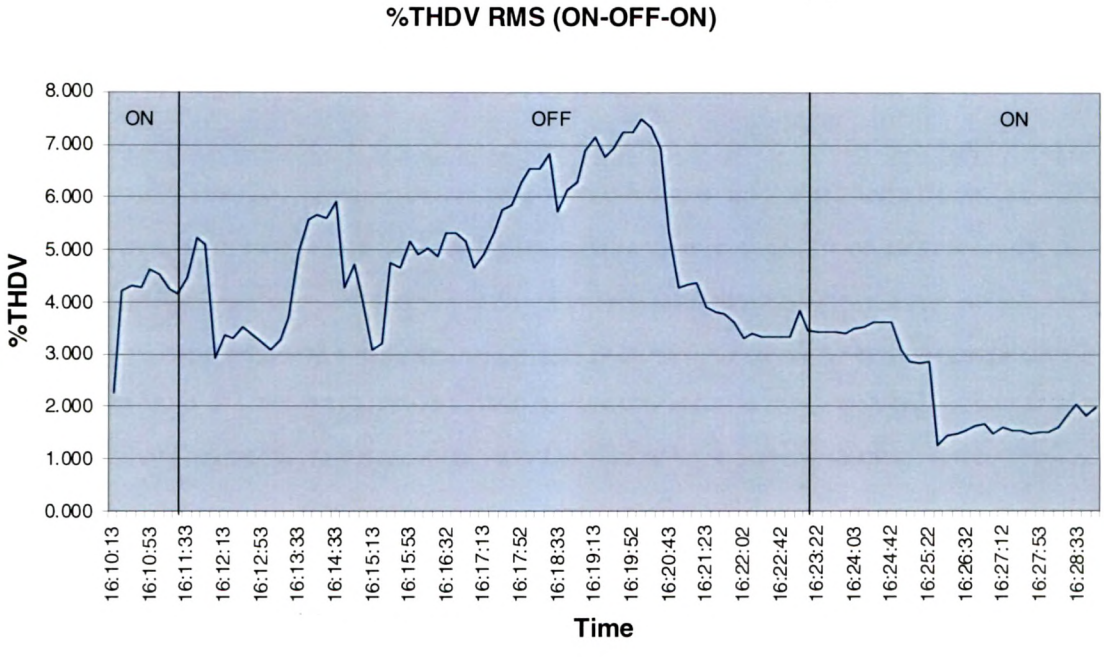


Fig. 4.31 Voltage THD variation with and without DRPC compensation

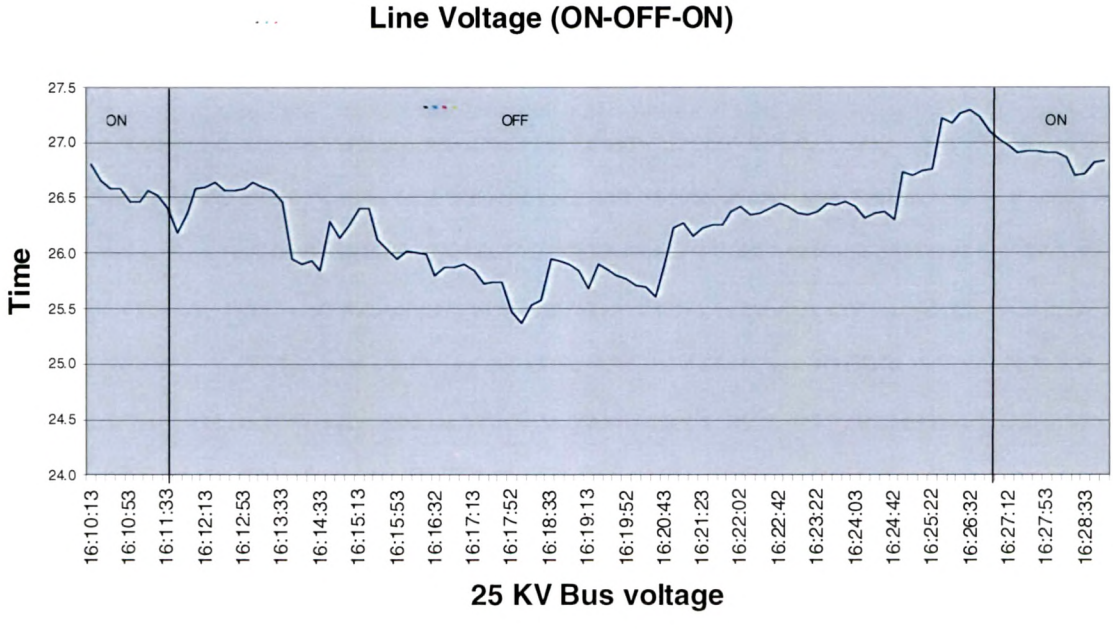


Fig. 4.32 Bus Voltage variation with and without DRPC compensation

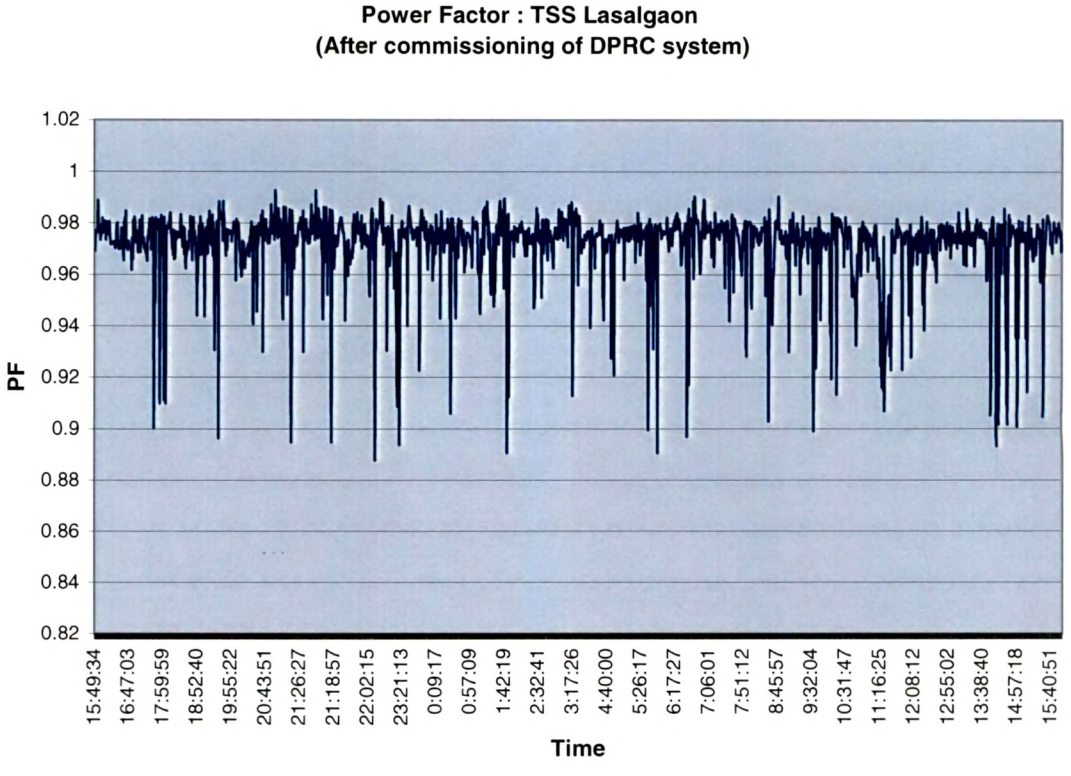


Fig. 4.33 Close to 0.98 power factor after installation of the DRPC system

The results show that the average monthly power factor has improved from 0.78 to 0.93-94, and there is a reduction in maximum 2000 – 2400 kVA apart from improving voltage by almost 750 - 1000 Volts.

The reduction in MVA by improving the power factor significantly reduces the incoming supply current, improves savings in electricity bill due to reduction in MVA (maximum demand), helps avoiding power factor penalty (or even rebate due to betterment of power factor wherever applicable). It also improves savings due to reduction of copper losses in the 132 / 25 kV transformers. Table 4.3 gives the improvement in power factor and reduction in kVA due to installation of DRPC.

Table-4.3: Performance of TSS
(before and after commissioning IGBT
based VSC type DRPC equipment)

Month' 05	PF	MD (kVA)	Reduction in kVA
Before Compensation			
Feb' 05	0.78	11840	
After Compensation			
April' 05	0.93	10680	1160
May' 05	0.92	10080	1760
June' 05	0.93	9480	2360
July' 05	0.94	9480	2360
Aug' 05	0.94	9840	2000

It should also be noted that the Voltage Source Converters (± 1200 kVAR connected on the secondary side of the 1.6 MVA transformer) assure no resonance with supply short circuit impedance. The Low Voltage (LV) side of the transformer with STATCON is free from ac capacitor and hence, it does not attract the traction load harmonics. The 1800 kVAR capacitor bank connected on the High Tension (HT) side with 13% series reactor (tuned at 2.77 of the fundamental frequency of 50 Hz) also does not attract any harmonics as it is tuned below the lowest order harmonics (3^{rd} harmonic) existing in 25 kV traction bus.

4.9.4 SUMMARY OF TSS STATCON INSTALLATION

To summarize, the STATCON based Dynamic Reactive Power Compensation (DRPC) system as described and as installed in TSS has resulted in following performance improvement for the Sub-Station.

- Real-time smooth power factor improved from 0.78 to minimum of 0.94
- Reduction of Maximum Demand by 2400 kVA
- Reduction of system losses (which need to be established based on the network components)
- Improvement in voltage profile by 750 – 1000 Volts, which helps to improve the Traction Power system stability

Since most of the Sub-Stations already have the Fixed HT de-tuned filter banks for power factor improvement, STATCON can be potential solution for DRPC system against use of TSC based system which demands removal of existing HT capacitor banks. Further, this approach also saves additional investment for the HT switchgear. Extended details are covered in [225].

4.10 EMI-EMC CONSIDERATIONS

Following points gives the vital notes as experienced from STATCON installation for achieving optimal performance and all round: 24hours-265 days availability of the system in the reffered installations. This learning experience can be considered as general guideline for engineering and field installation of any of such power converter based solution.

4.10.1 CARE IN POWER STACK AND GATE DRIVE INTEGRATION

i. IGBT modules are mounted on the heat-sink in such a way that the heat dissipation is evenly spread.

ii. Glass coated sleeves are used for R-C-D connections to avoid insulation failure and enhance thermal withstanding

iii. Twisted pair for Gate - Emitter connections are used with minimum lengths.

iv. The entire power stack is enclosed in a sheet metal box to avoid EMI interference with control electronics.

v. Separate R-C filter is provided per phase to filter the switching frequency ripple and associated noise.

vi. Control electronic and the gate drive card(s) inputs are integrated using flat cables as removable connectors so that assembly is easy.

vii. Control electronics power supplies (5V, +/-12V, +/-15V) used are linear power supplies contained in a separate housing. SMPS design is avoided due to EMI effect.

viii. Control electronics PCBs are integrated in such a way that the interconnection length for the flat cables is minimal.

ix. Certain amount of the time delay in the converter operation is introduced after the operation of each contactor to ensure that the electromagnetic ambient is stabilized within the cubicle and controls are not disturbed.

x. Sufficient amount of isolation is provided between low and high voltage areas on the gate drive cards.

xi. Sandwich construction of bus-bar facilitating in reduce bus-bar inductance and facilitating desired isolating voltage levels with minimal gate drive connection lengths is preferred.

4.10.2 CARE IN CONTROL HARDWARE AND SOFTWARE DESIGN

i. Select Digital Processor with internal PLL(Phase Lock Loop) so that internal clock frequency for processing can be higher , however, outside frequency can be low and there by minimizing effect of noise coupling as well as generation.

ii. Use controller clock frequency based on the desired performance (avoid higher clock speeds just for the sake of it).

iii. Use small filter chokes and Tranzorbs at the interfacing points so as to dampen the effect of high frequency conducted noise on signal paths.

iv. Use of watchdog timer at the controller level for graceful recovery of the system under undesirable conditions.

v. Have effective combination of hardware and software filtering for interfacing signals. It is very important that apart from normal operating frequency under consideration, the signals are sampled such that the noise impact due to Surge, EFT, ESD test duties are effectively eliminated.

vi. Software check on the acquired parameters, to ensure that, they are within limits. These limits can be dynamically set during operation.

vii. Unused interrupts on the digital processor to be masked and also used interrupts to be selectively enabled during the program flow.

viii. The unused pins on the controller and associated peripherals to be appropriately pulled low/ pulled high so as to prevent unwanted noise coupling on the signal paths.

ix. Use of schmitt gates or waveform shaping circuits is always advisable so that digital gates do not see slowly varying inputs and start seeing logical signals as analog inputs/outputs.

x. For critical signals use either redundancy or have hardware plus software based logic determination.

4.10.3 CARE FOR SIGNAL CONDITIONING AND ANALOG SECTION

i. When common- differential mode filtering capacitors or choke are deployed on incoming line, neutral, earth paths, it is very important that tolerances of the filter components is not wide, else the conversion of common mode signal into differential and vice versa can happen.

ii. Suitable R-C filter are recommended, to filter the switching frequency ripple and associated noise for the power supply feeding the analog section.

iii. Each signal before being subjected for analog to digital conversion is recommended to be band limited based on application. If possible, suitable soft filtering techniques like Discrete Fourier Transform (DFT) can be deployed for extracting the signal values at the desired frequency.

iv. Very effective segregation between analog and digital section, and similar between low power and high power section is important. It should be noted that each feeding connection or track should have associated return path.

v. Suitable RC filters or LC filters needs to be deployed when signals are being driven over length to ensure effective waveform shaping.

vi. It is recommended that only single point interconnection in the design should exist for the analog and digital section ground. And this interconnection preferably should be nearest to the most sensitive section of the design, typically ground connection of analog to digital converter. This single point should also get coupled to the earthed chassis of the equipment with the shorted path using metal contact, to ensure that it remains at the most stable potential irrespective of any disturbances traveling on the lines or present in given Radio Frequency (RF) environment.

vii. For control electronics power supplies if design/power consumption limits permits, then linear power supplies are recommended. If SMPS are deployed, transformer design with shields is important and special inductive filter on the output path needs to be suitably deployed.

viii. The entire power supply should be very closely coupled to the solidly earthed equipment enclosure which is preferred to be metallic.

ix. Front interface – Current Transformers (CTs) / Magnetic parts producing strong magnetic field at higher operating currents are preferred to be mounted in a separate subsection and if possible with shortest return path to the earthed equipment chassis.

x. R- Core transformer(s) with 3 shields to minimize stray coupling capacitance effect between primary and secondary windings should be preferred. First shield is connected to primary return path, second to earth and third to the secondary return path. R Core transformer usage gives low flux leakage.

xi. Transformer secondary are connected to the power supply Printed Circuit Board (PCB) / control PCB through twisted wires.

4.10.4 CARE IN THE PCB DESIGN STAGE

i. Before the hardware design is taken up for engineering, earthing scheme for the design is must to be arrived at.

ii. Split of the functional design due to product engineering requirements, should ensure that for each interconnection among the PCBA, adequate return path and ground lines are incorporated. This means that for "x" no. of signals, "x" return path is also considered.

iii. Running of ground lines adjacent to the high frequency signal lines to minimize coupling problems is desired.

iv. Extreme care has been taken during the PCB design stage to reduce the coupling noise, reduced track lengths, use of buffer amplifiers at every input/output stage, use of power supply decoupling capacitors for Integrated Circuits (ICs) to suppress the high frequency noise, and separate peripheral loop for earth connection. One can use multilayer PCBs to incorporate power supply and signal ground planes for better performance.

v. Usage of via's, through hole connects or long track lengths for the sensitive signals (for e.g. processor clock, reset) should be kept absolutely minimum.

vi. Crossover of analog signals over digital planes also should be avoided.

vii. Component placement should also be conceived in the same way as the direction of intended flow or expected action. For .g. filter elements should be seen first on the path and then the functional circuit and not vice versa even though all the elements are connected to the same node.

viii. Looping of analog ground/ digital ground is fully avoided when PCB designs are implemented.

ix. Signal getting connected to high impedance circuits should be ensured to have the smallest length.

4.10.5 CARE AT THE PRODUCT ENGINEERING LEVEL

i. Power devices used in the power supply if mounted on the heat sink, should be such that the heat dissipation is evenly spread and does not affect thermally the sensitive components in the analog section.

ii. Twisted pair wires for interconnections are used with minimum lengths.

iii. Openings, joints in the enclosure have to be at minimum. For ease of manufacturing even if the metallic enclosure makes uses of different section, it is important that joints deploy very effective spreaded conductive interconnects.

iv. Gaskets if used for facilitating ingress protection requirements between metallic joints should be conductive type only and insulating type has to be strictly avoided.

v. Rusting or painted surface for the metallic joints is to be strictly avoided.

vi. If the enclosure is of plastic for aesthetic reasons, it is recommended that it still makes use of earthed metallic chassis. It is also recommended that plastic with internal metallisation could be better approach for effective EMI mitigation.

vii. Any overlay used in the front for keypad, LCD window should avoid any directly exposed metal part. It is also preferred that conducting substrate/ wire mesh is used at the back of

overlay to offer homogenous equi-potential surface for the electronics inside the control cabinets.

viii. Line filter if deployed on the incoming requires seeing the direct connection to the cabinet chassis so as to give shortest return path to the incoming high frequency noise.

ix. It should be noted that design needs to avoid usage of long cables for the return path either for power supply or signals, from any given PCBA or between inter PCBA. Especially, the paths which are likely to carry high frequency current components needs to be supported by braided conductors or metallic strip rather than wired cables. It is to be noted that extra length of wire which meets the functional performance at the power frequency, can create serious difficulties for the electronics response to the noise and has to be strictly avoided.

x. Control electronic if are integrated using flat cables for ease of assembly, needs to ensure that unnecessary length of wires to support the ease of assembly is to be strictly avoided.

4.10.6 CARE AT THE INSTALLATION LEVEL

i. Shielded cables are preferred while feeding the analog, communication interfaces to the converter panel. The shield also is desired to get connected to the panel chassis directly at the point of entry with suitable provision for shield termination.

ii. Additional bonding conductor over entire length of CT and potential transformer (PT) control cables preferably to be used as that is the major source of primary and secondary voltage levels likely integration.

iii. Mix up of low voltage (signal and control) cables and power cables are completely avoided. It is preferred to use separate cable trays while handling such signals.

iv. Lugs or cable shoe are recommended to be made use of and it is important full 360 deg. mating is taken care of.

v. Instead of single conductor, it is better that multicore conductors are deployed for the signals which are expected to carry high frequency components, so as to reduce the impact due to skin effect.

vi. For the control cubicle of switchgears, neutral and earthing are to be fully separated. The earth connections are provided from a separate busbar in the cubicle to various points which include heat sink, power stack housing, cooling fans etc.

vii. Each power and control contactor, ac coil is to be provided with an R-C snubber network.

viii. Instead of single transformer having multiple taps on secondary, different transformers for specific voltage supplies are used. This reduces inter supplies noise coupling.

ix. Control electronics power supply is taken from the phase different then the phase used for ac control contactors, fans, blower etc. to reduce interference with the control electronics circuits.

x. If required, the individual component / module arrangement and the wire routing has been iterated number of times for optimizing the reduction in EMI effect.

Re-engineered STATCON panel for Site installation addressing the design care are shown in fig 4.34.

Fig. 4.34 Re-engineered STATCON

Extended details are covered in [226].

4.11 CONCLUSION

As highlighted in the chapter, there have been many technological alternatives for implementing the Digital core control (Hardware + Firmware) but simply achieving functional performance in the laboratory environment is not sufficient enough to guarantee the performance in the field. Considerable engineering aspects, as highlighted in the chapter forms the backbone and are required to be addressed when the performance on the field is to be guaranteed. This experience has been very clearly brought out with automobile and railway installations as reference while detailing out the critical aspects for highly reliable operation.